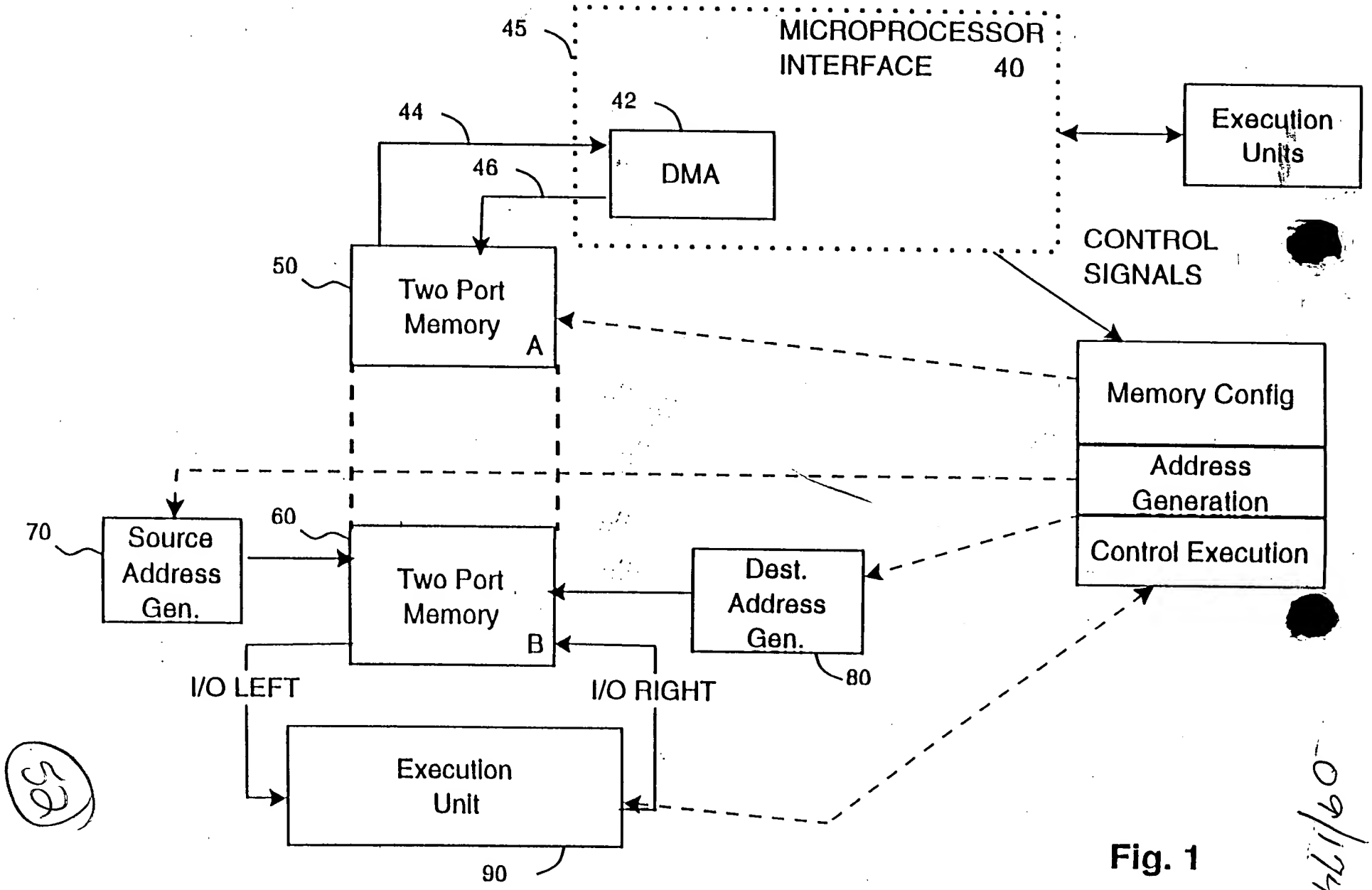

45
MICROPROCESSOR
INTERFACE 40
44
42
DMA
Execution
Units
46
CONTROL
SIGNALS
50
Two Port
Memory
A
Memory Config
Address
Generation
Control Execution
70
Source
Address
Gen.
60
Two Port
Memory
B
Dest.
Address
Gen.
80
I/O LEFT
I/O RIGHT
Execution
Unit
90

Fig. 1

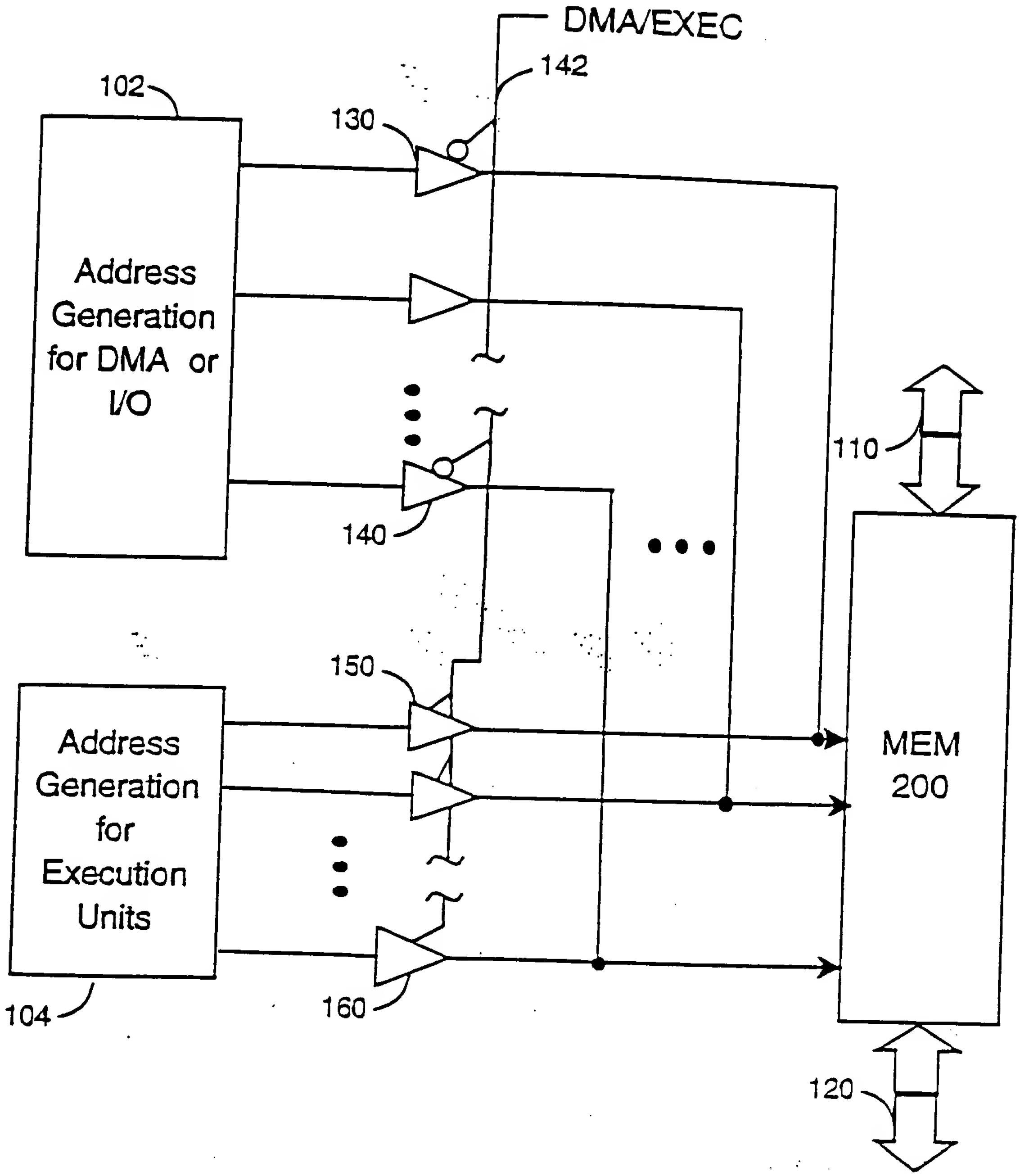

DMA/EXEC
142
102
130
Address Generation for DMA or I/O
110
140
150
Address Generation for Execution Units
MEM 200
104
160
120

FIG. 2

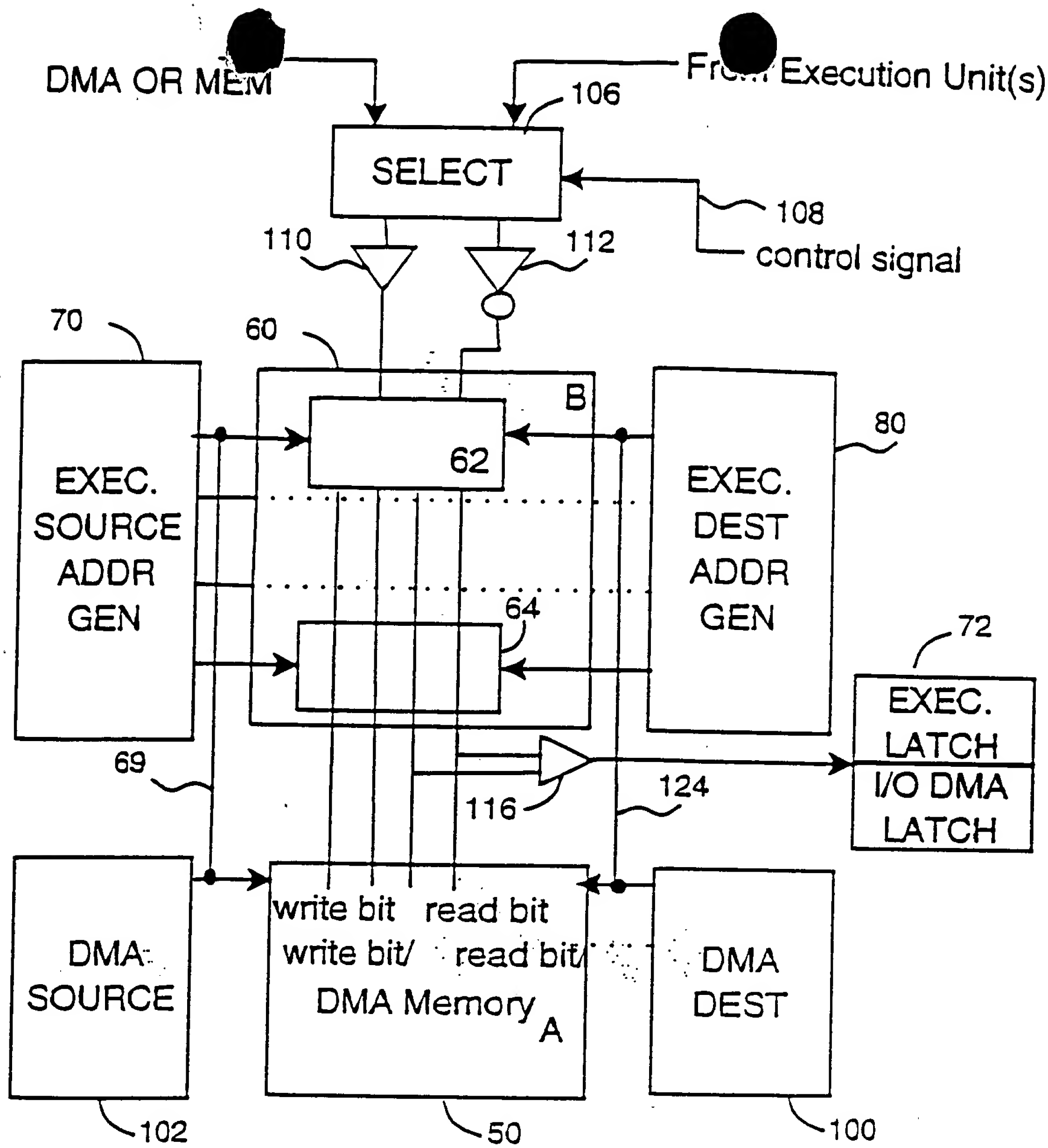

DMA OR MEM
Execution Unit(s)
106
SELECT
108
control signal
110
112
70
60
B
80
62
EXEC.
SOURCE
ADDR
GEN
EXEC.
DEST
ADDR
GEN
64
72
EXEC.
LATCH
I/O DMA
LATCH
69
124
116
write bit
read bit
write bit/
read bit/
DMA Memory
A
DMA
SOURCE
DMA
DEST
102
50
100

Fig. 3

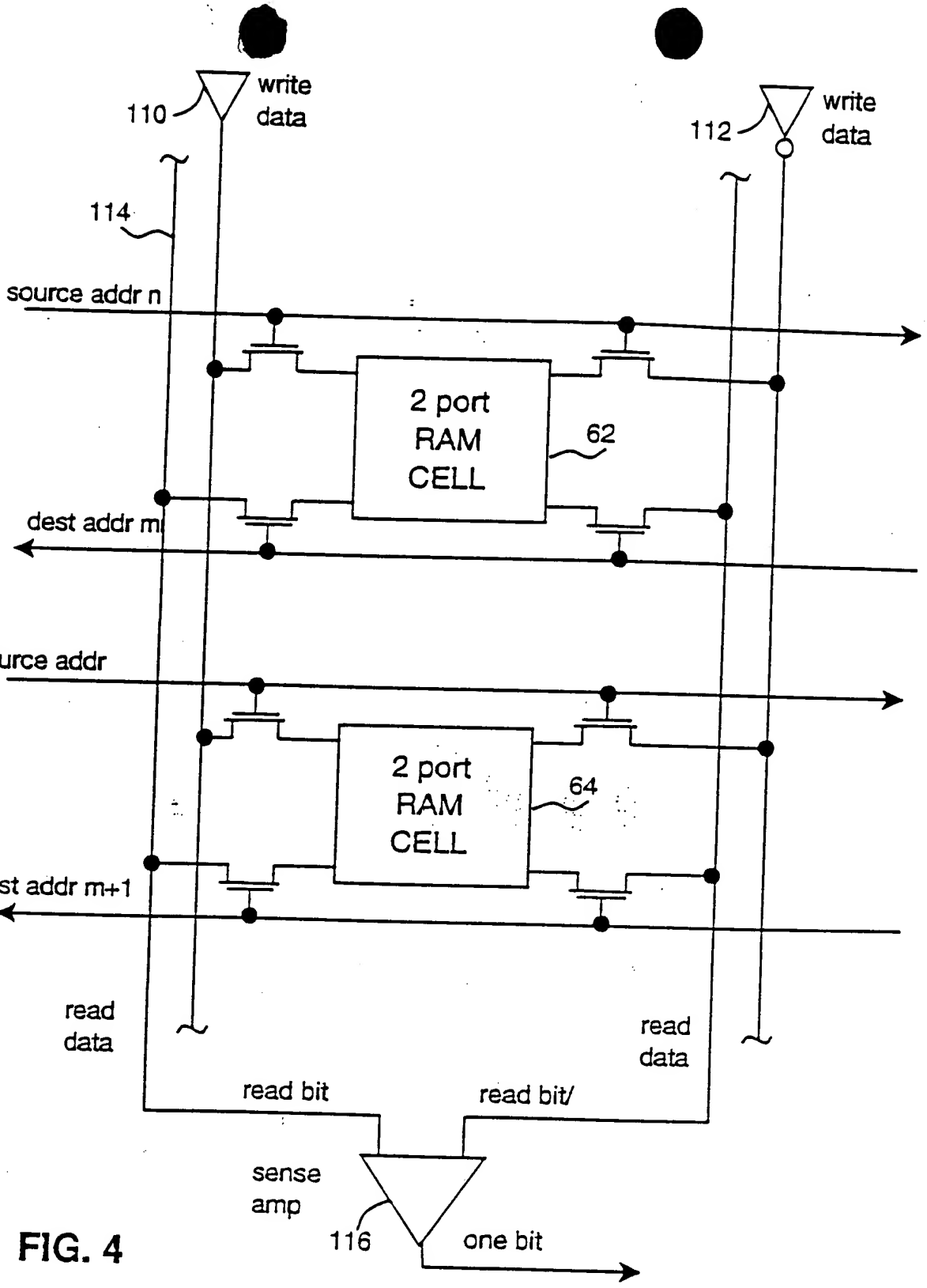

write
data
110
write
data
112
114
source addr n
2 port
RAM
CELL
62
dest addr m
source addr
2 port
RAM
CELL
64
dest addr m+1
read
data
read
data
read bit
read bit/
sense
amp
116
one bit

FIG. 4

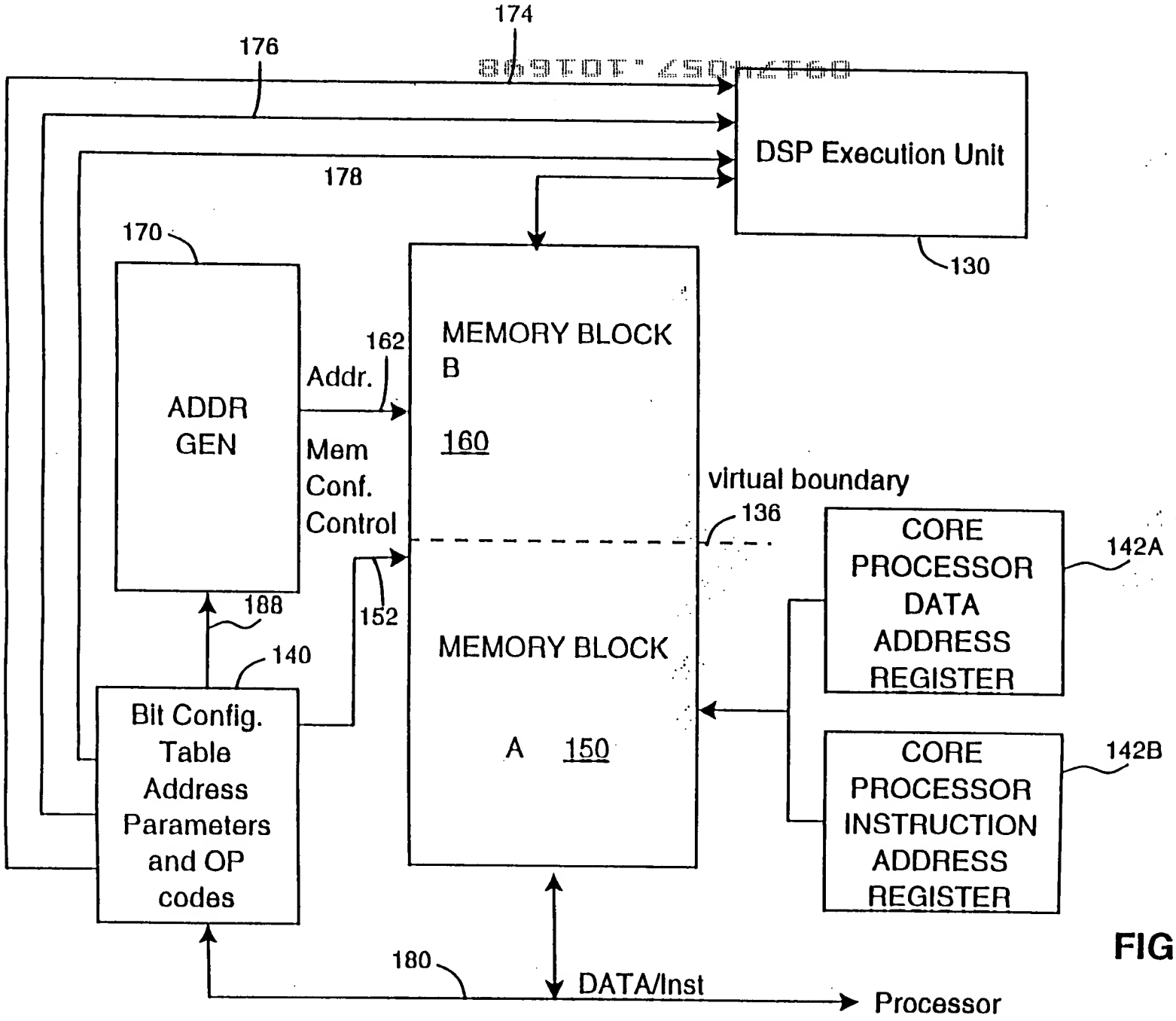

174
176
DSP Execution Unit
178
130
170
ADDR GEN
162
Addr.
Mem Conf. Control
MEMORY BLOCK B
160
virtual boundary
136
CORE PROCESSOR DATA ADDRESS REGISTER
142A
188
152
140
MEMORY BLOCK A 150
Bit Config. Table Address Parameters and OP codes
CORE PROCESSOR INSTRUCTION ADDRESS REGISTER
142B
180
DATA/Inst
Processor

FIG. 5A

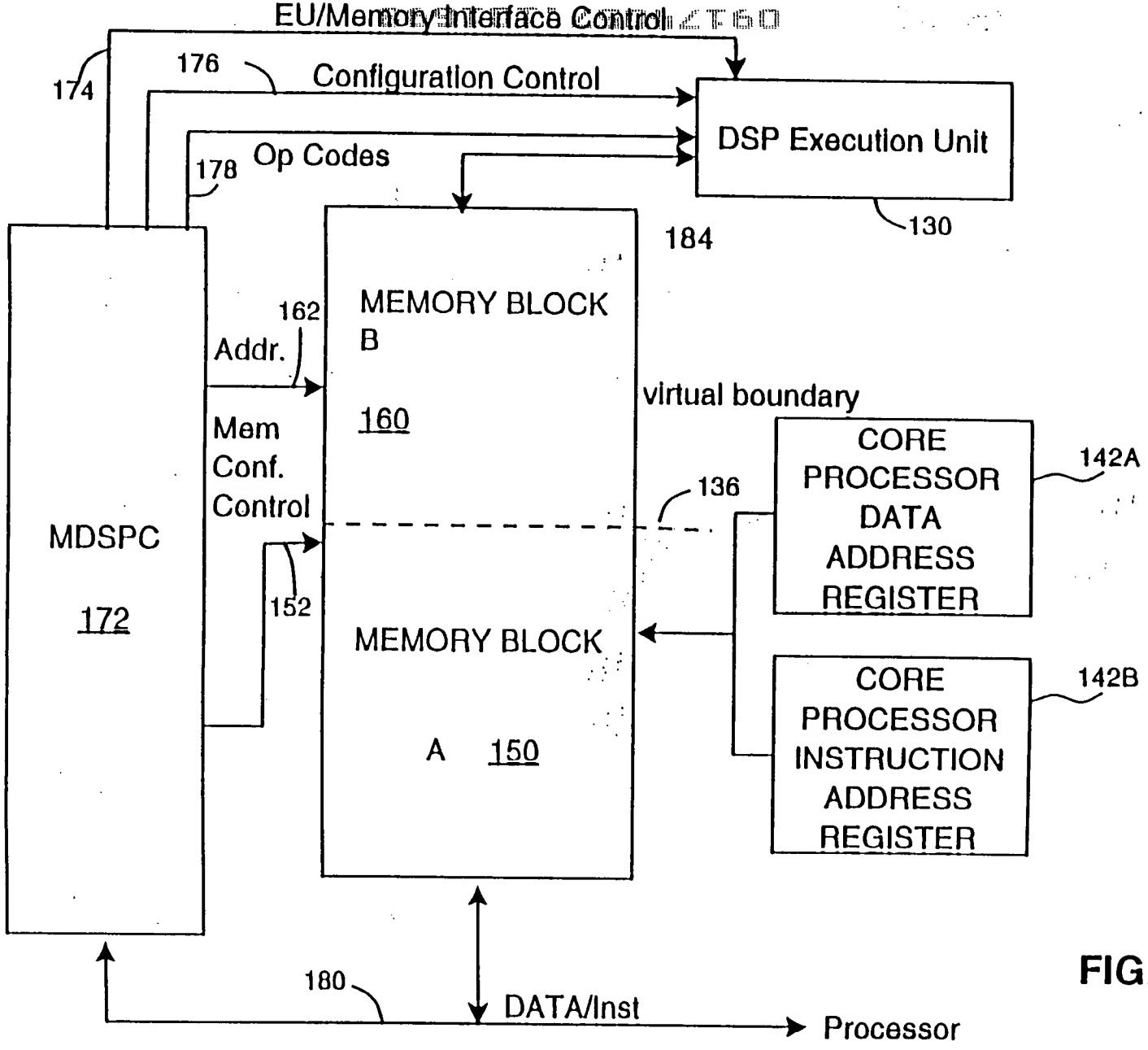

EU/Memory Interface Control
174
176
Configuration Control
DSP Execution Unit
178
Op Codes
130
184
MEMORY BLOCK
B
162
Addr.
160
virtual boundary
Mem
Conf.
Control
136
CORE
PROCESSOR
DATA
ADDRESS
REGISTER
142A
MDSPC
172
152
MEMORY BLOCK
A 150
CORE
PROCESSOR
INSTRUCTION
ADDRESS
REGISTER
142B
180
DATA/Inst
Processor

FIG. 5B

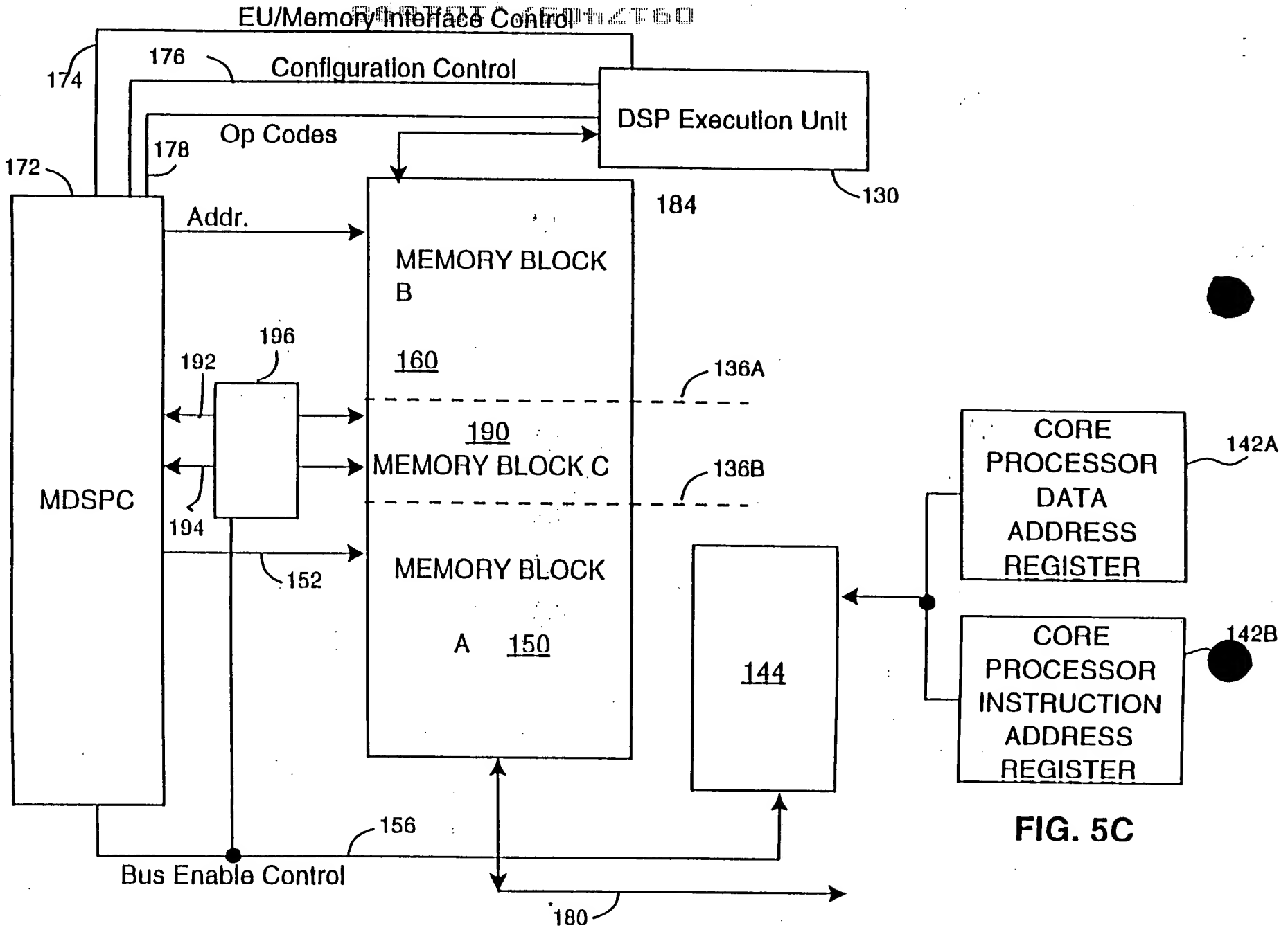

EU/Memory Interface Control
174
176
Configuration Control
DSP Execution Unit
Op Codes
178
172
184
130
Addr.
MEMORY BLOCK B
160
196
192
136A
190
MEMORY BLOCK C
136B
MDSPC
194
152
MEMORY BLOCK A 150
144
CORE PROCESSOR DATA ADDRESS REGISTER
142A
CORE PROCESSOR INSTRUCTION ADDRESS REGISTER
142B
156
Bus Enable Control
180

FIG. 5C

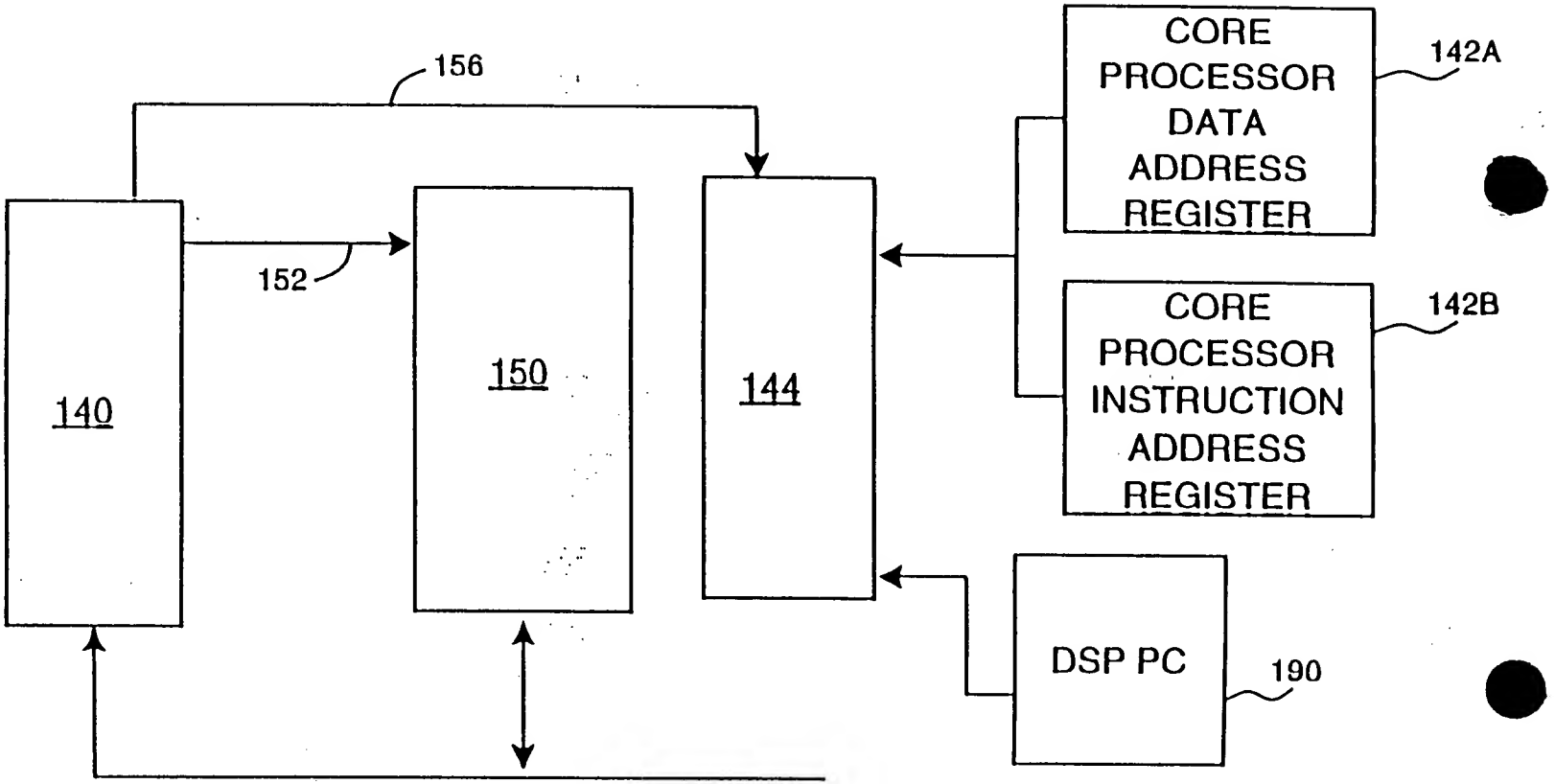

156
152
140
150
144
CORE PROCESSOR DATA ADDRESS REGISTER
142A
CORE PROCESSOR INSTRUCTION ADDRESS REGISTER
142B
DSP PC
190

FIG. 6A

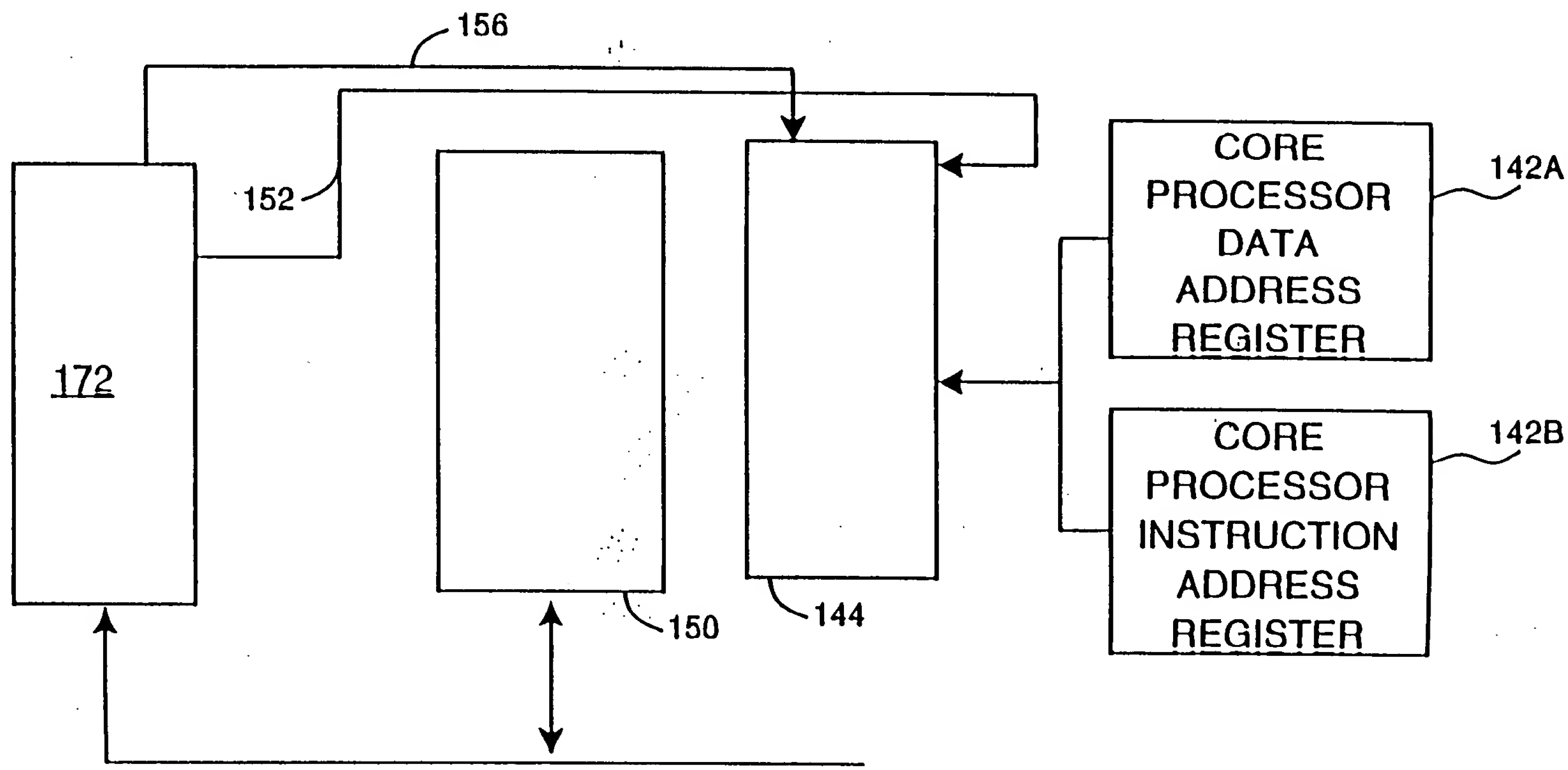

156
152
172
150
144
CORE PROCESSOR DATA ADDRESS REGISTER
142A
CORE PROCESSOR INSTRUCTION ADDRESS REGISTER
142B

FIG. 6B

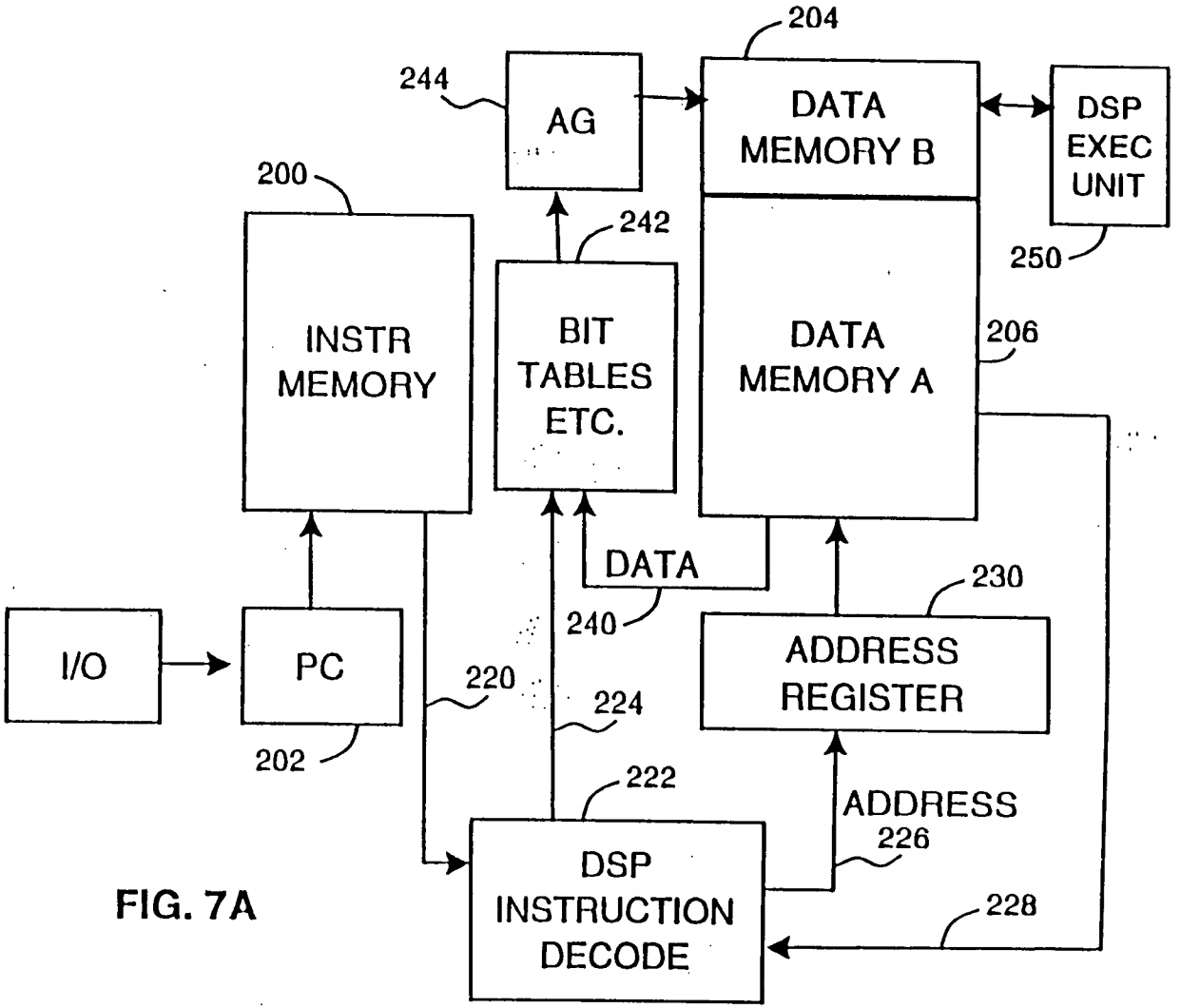


FIG. 7A

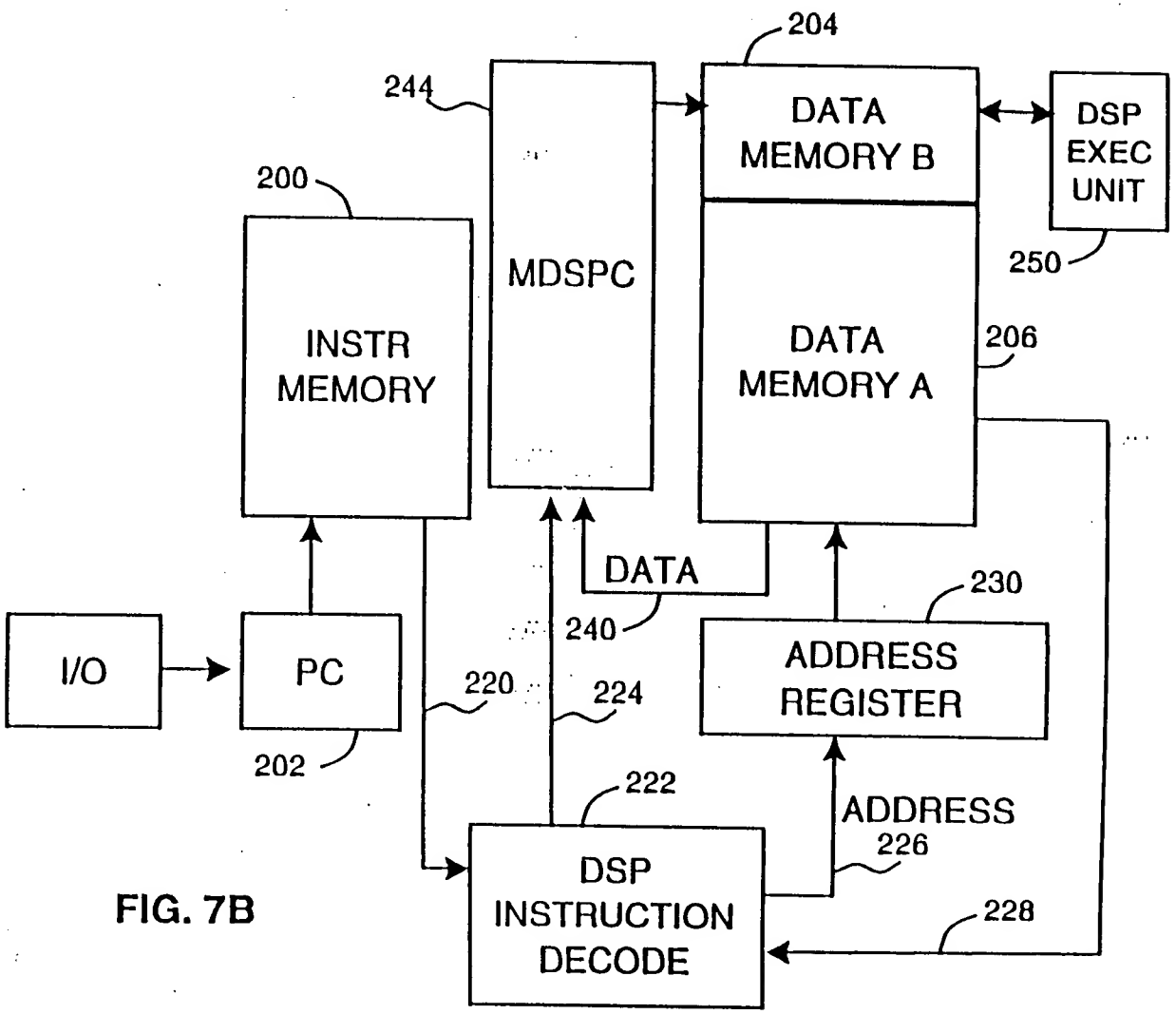


FIG. 7B

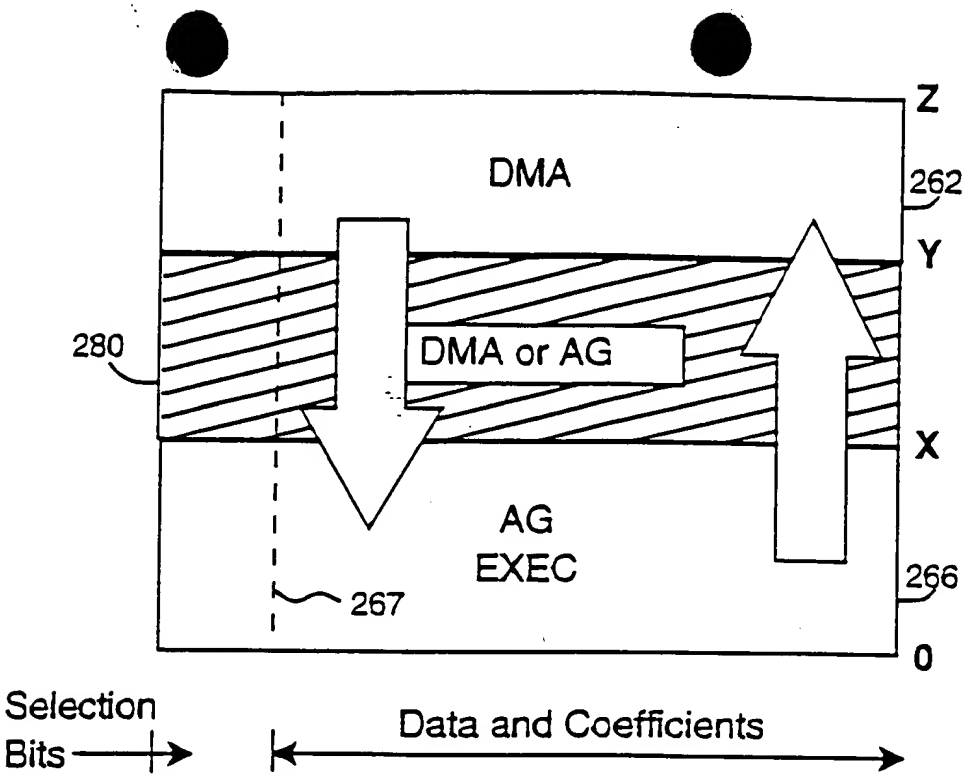


FIG. 8

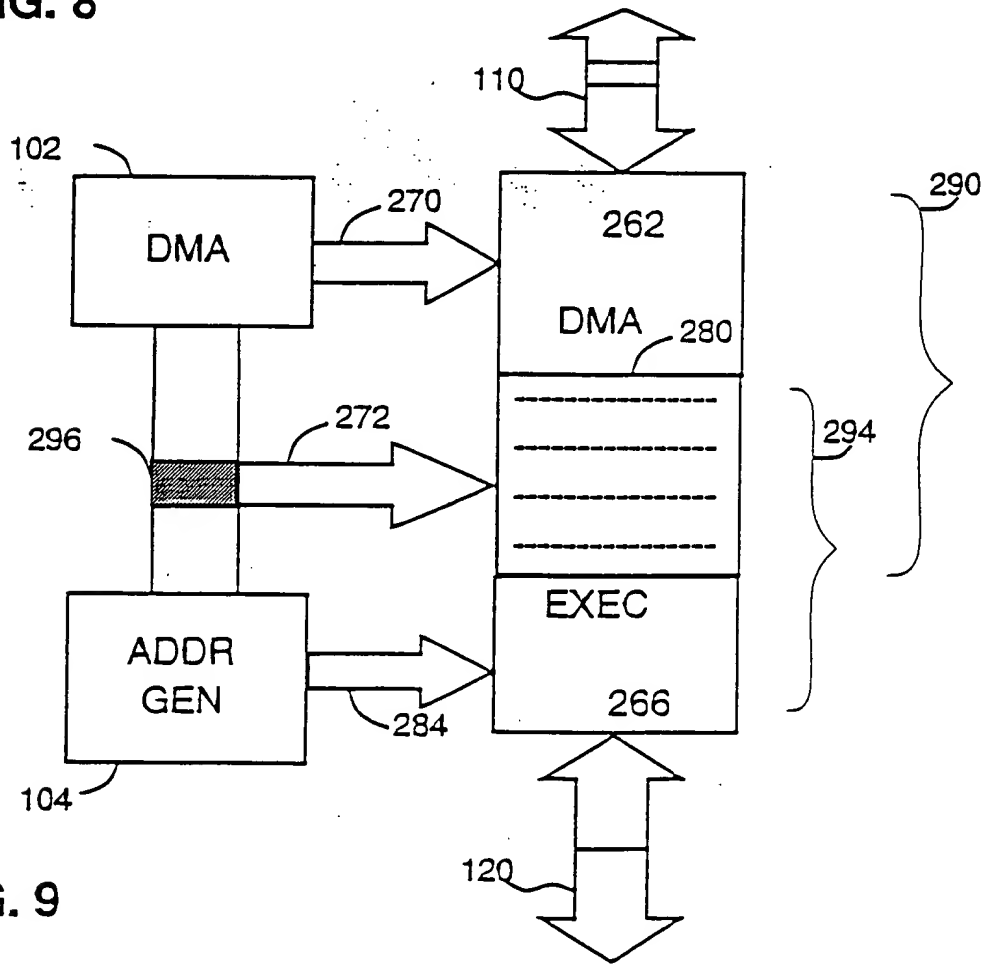


FIG. 9

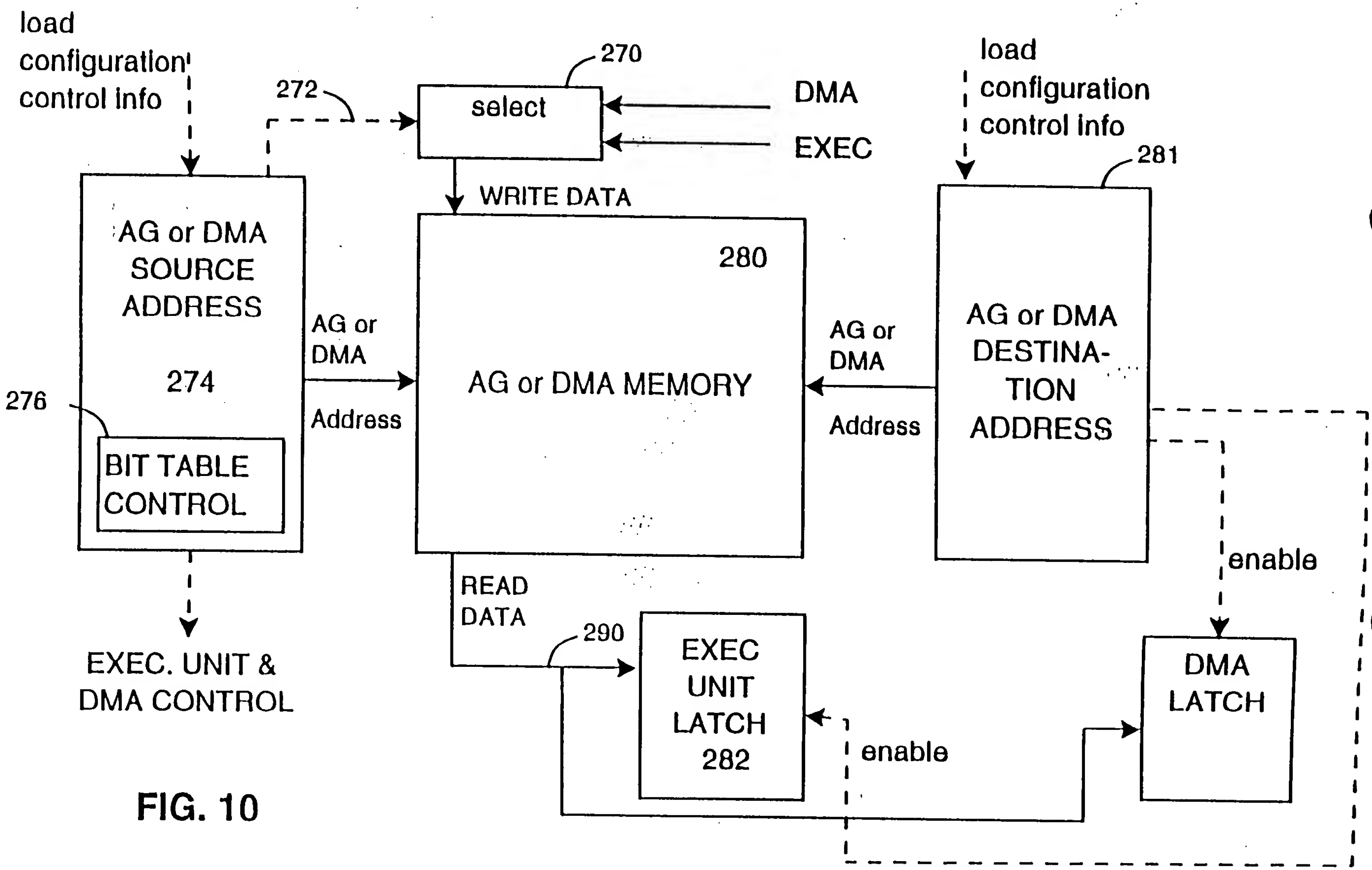

load configuration control info
272
270
select
DMA
EXEC
load configuration control info
281
AG or DMA SOURCE ADDRESS
274
276
BIT TABLE CONTROL
AG or DMA
Address
WRITE DATA
280
AG or DMA MEMORY
AG or DMA
Address
AG or DMA DESTINA-TION ADDRESS
enable
READ DATA
290
EXEC UNIT LATCH
282
enable
DMA LATCH
EXEC. UNIT & DMA CONTROL

FIG. 10

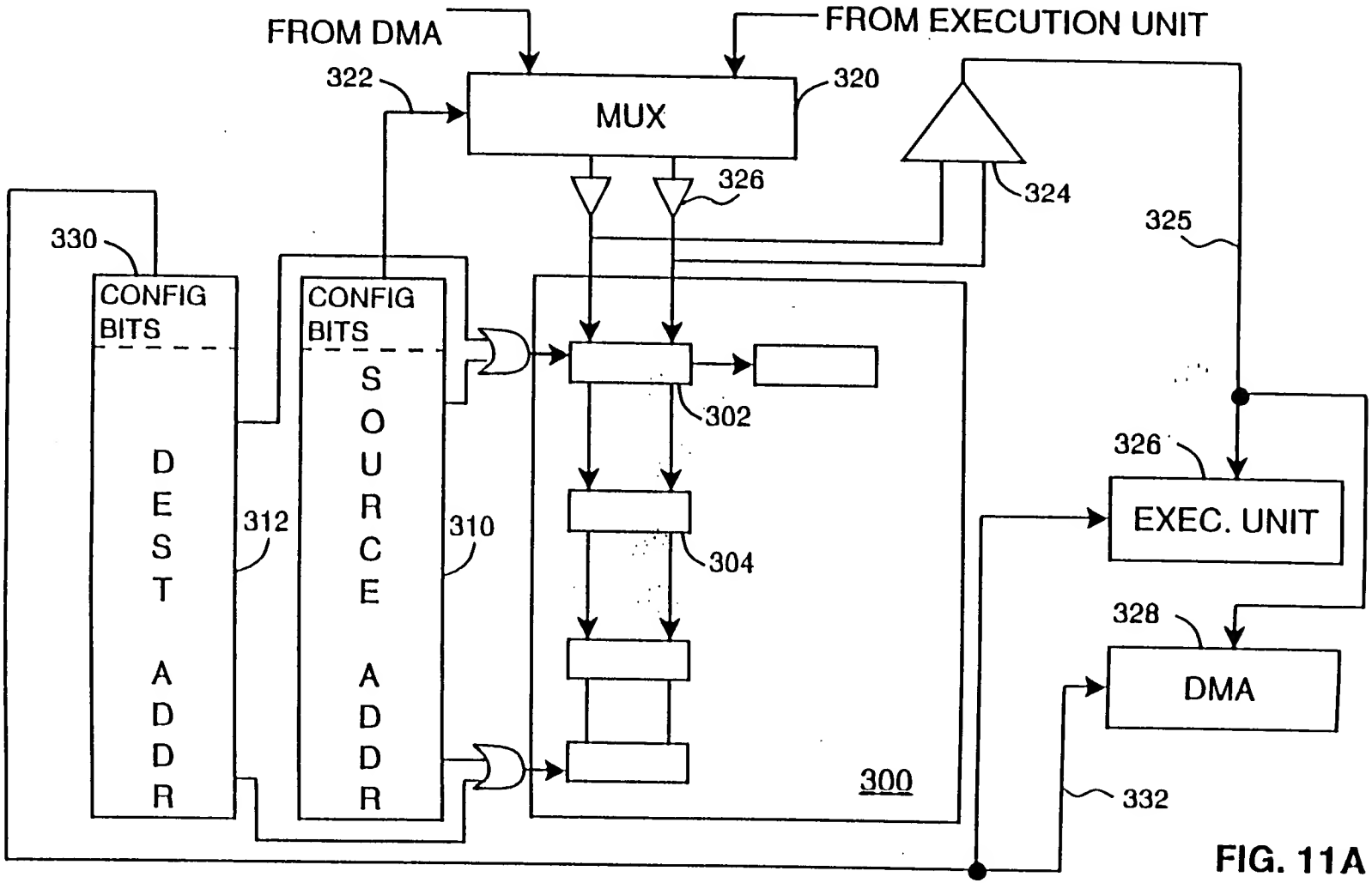


FIG. 11A

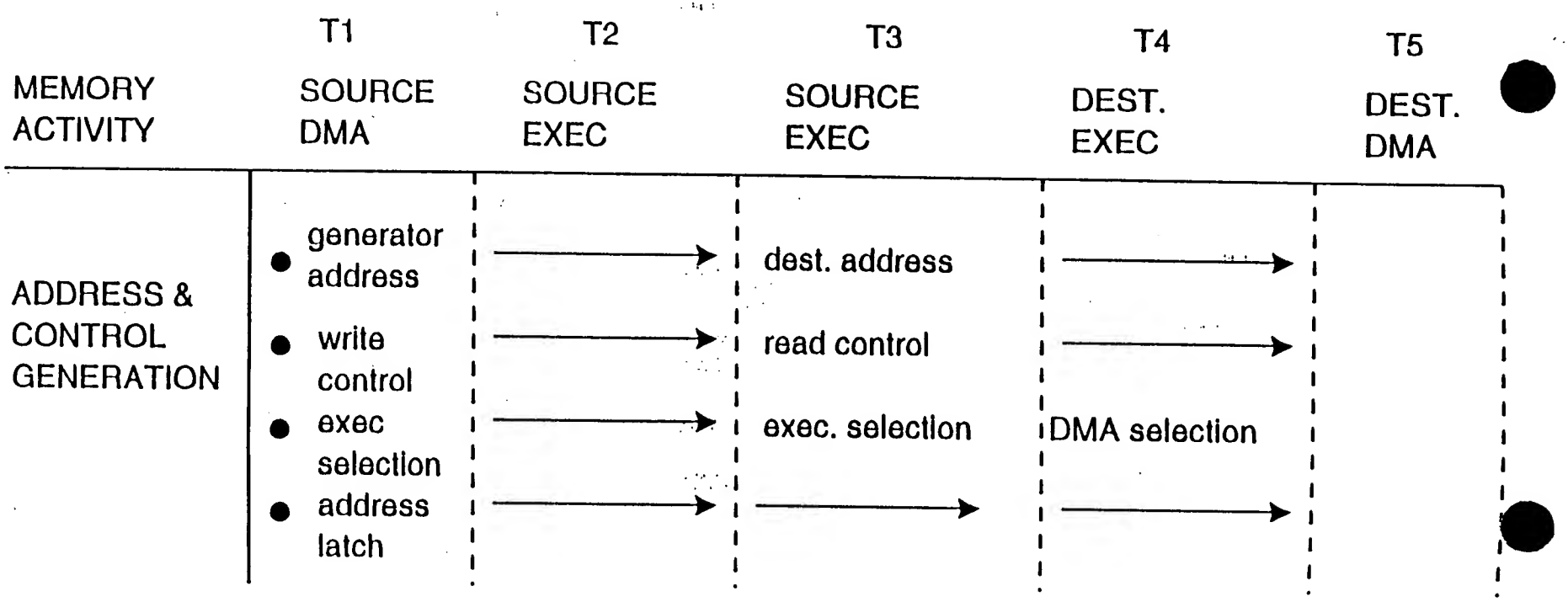


FIG. 11B

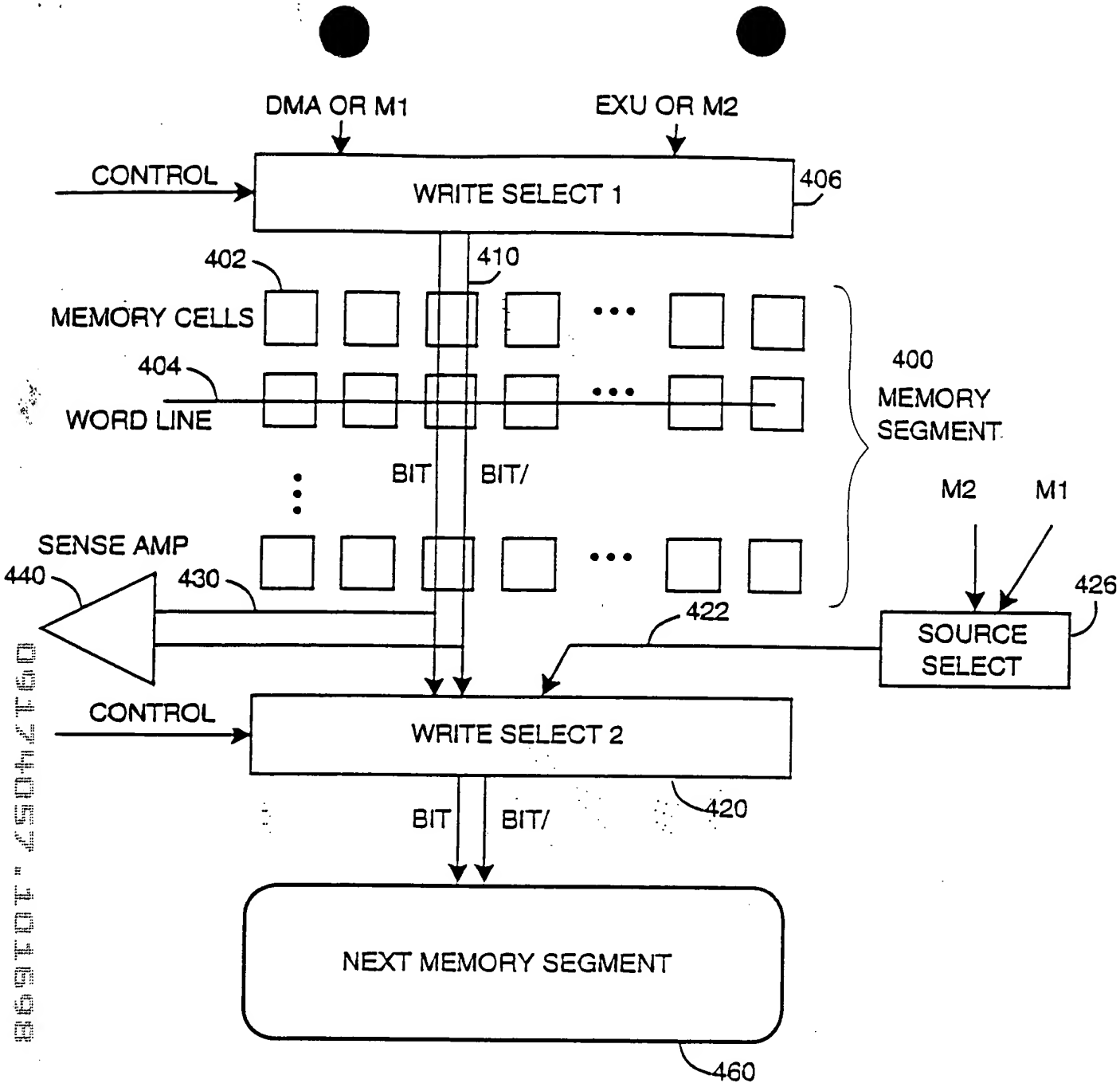

DMA OR M1
EXU OR M2
CONTROL
WRITE SELECT 1
406
402
410
MEMORY CELLS
404
WORD LINE
400
MEMORY
SEGMENT
BIT
BIT/
M2
M1
SENSE AMP
440
430
426
422
SOURCE
SELECT
CONTROL
WRITE SELECT 2
420
BIT
BIT/
NEXT MEMORY SEGMENT
460

FIG. 12

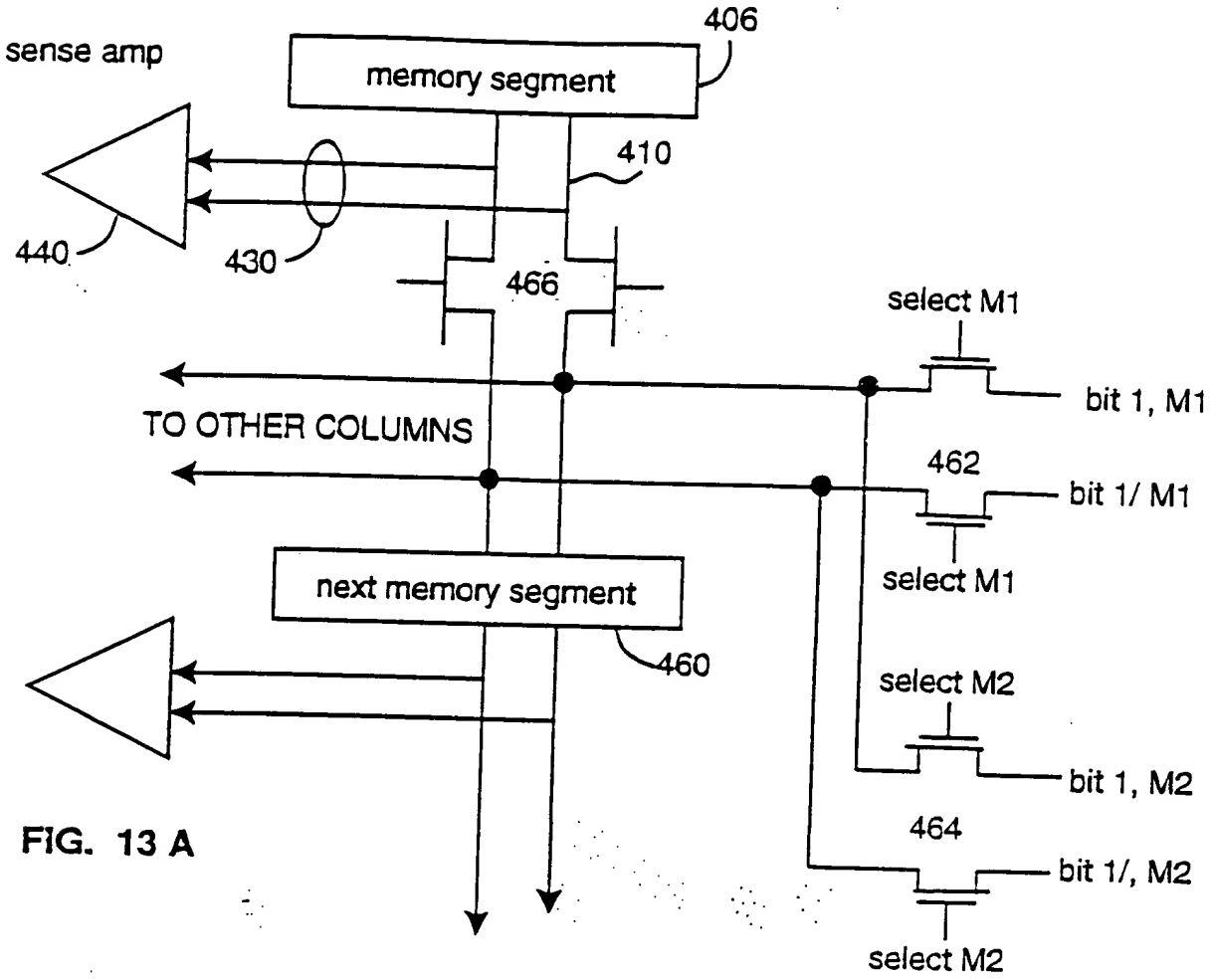


FIG. 13 A

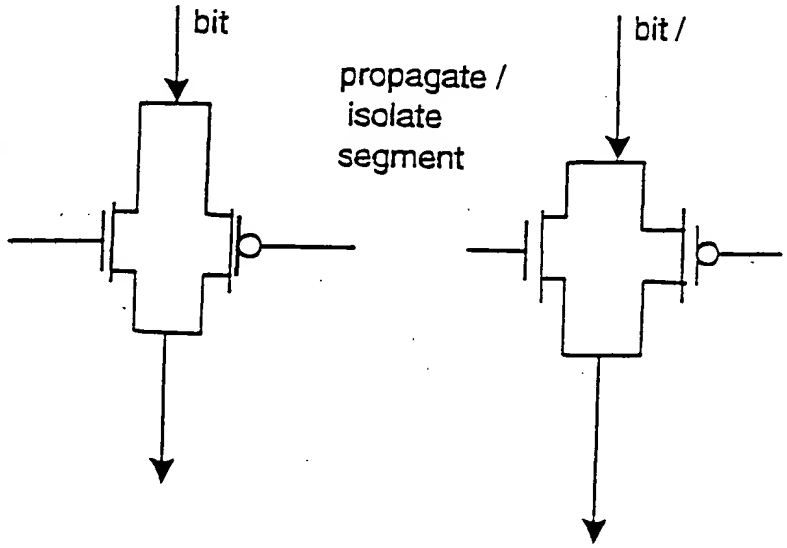


FIG. 13 B

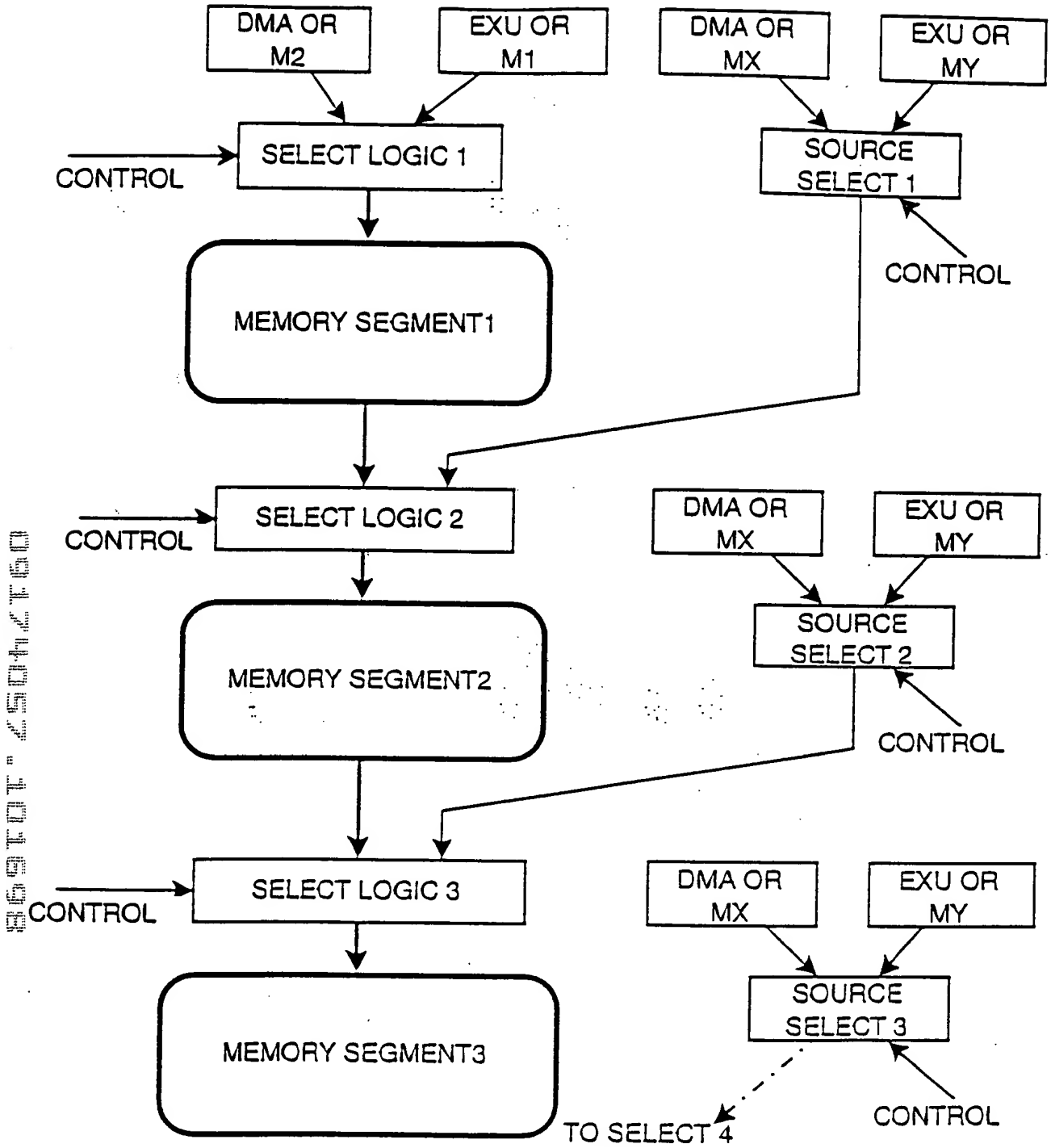

DMA OR M2
EXU OR M1
DMA OR MX
EXU OR MY
SELECT LOGIC 1
CONTROL
SOURCE SELECT 1
CONTROL
MEMORY SEGMENT1
SELECT LOGIC 2
CONTROL
DMA OR MX
EXU OR MY
SOURCE SELECT 2
MEMORY SEGMENT2
CONTROL
SELECT LOGIC 3
CONTROL
DMA OR MX
EXU OR MY
SOURCE SELECT 3
MEMORY SEGMENT3
TO SELECT 4
CONTROL

FIG. 14

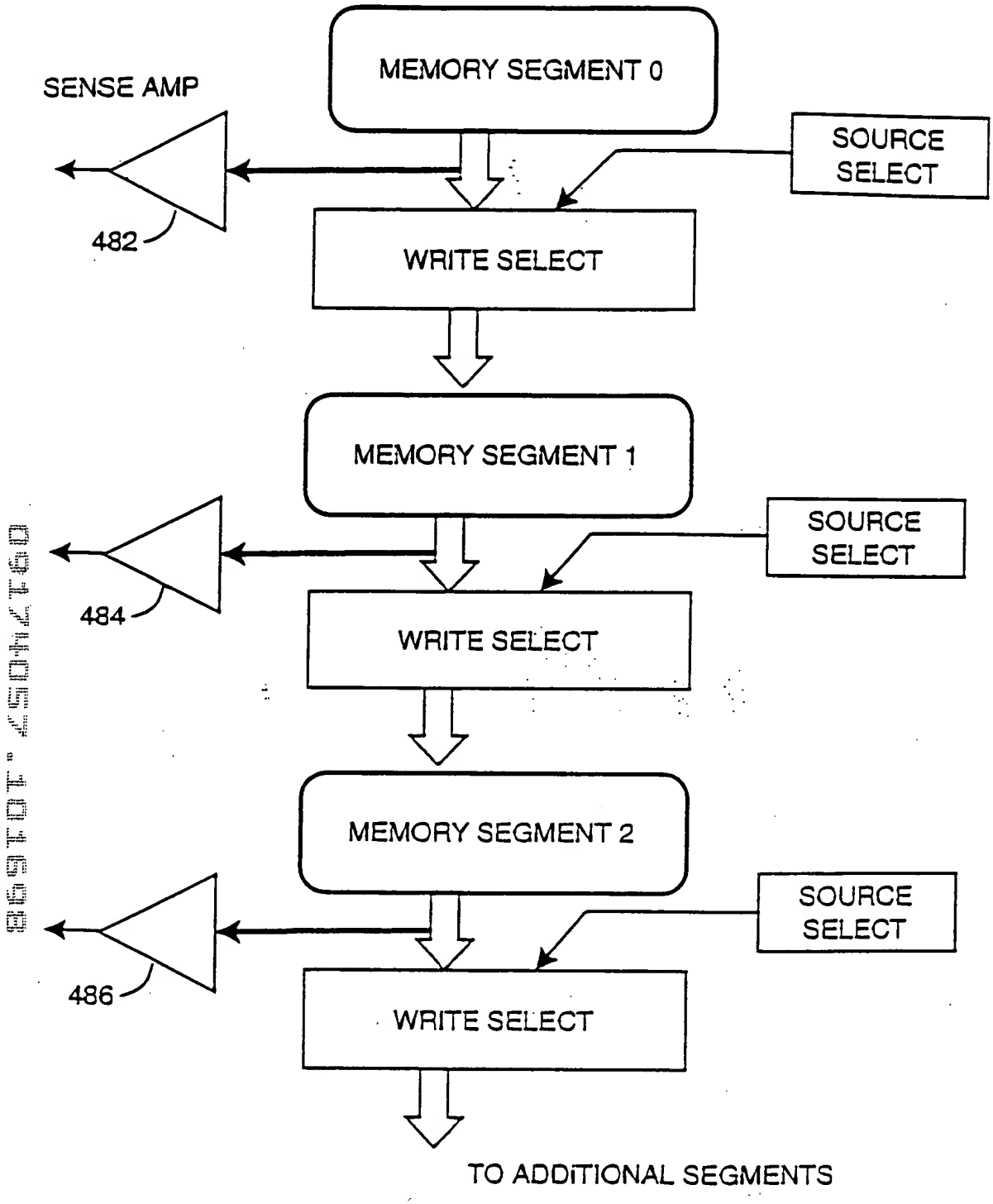

MEMORY SEGMENT 0
SENSE AMP
SOURCE SELECT
482
WRITE SELECT
MEMORY SEGMENT 1
SOURCE SELECT
484
WRITE SELECT
MEMORY SEGMENT 2
SOURCE SELECT
486
WRITE SELECT
TO ADDITIONAL SEGMENTS

FIG. 15

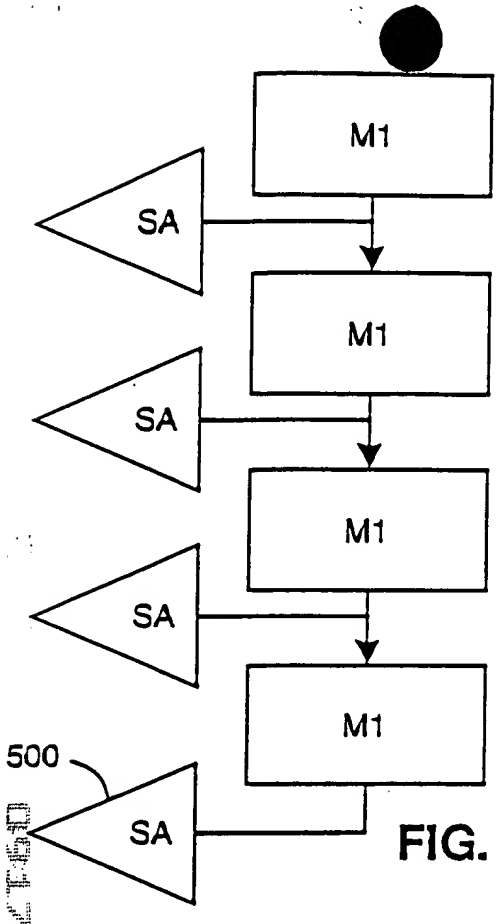


FIG. 16A

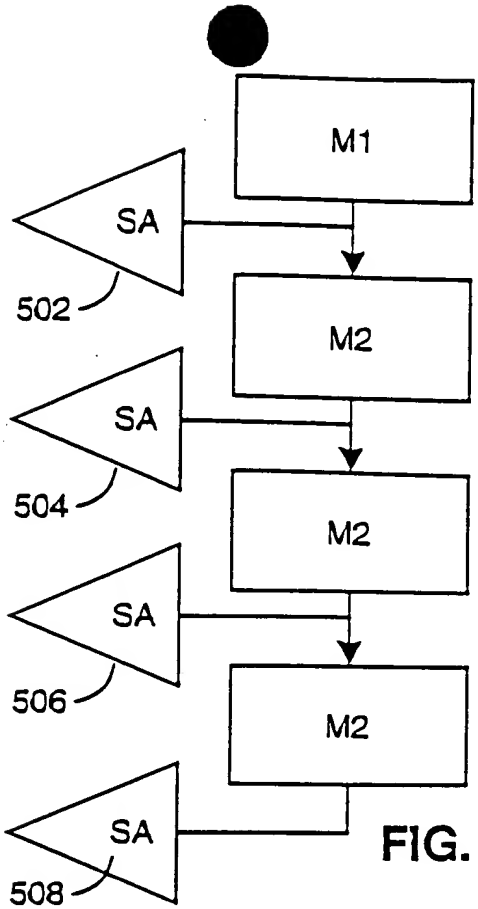


FIG. 16B

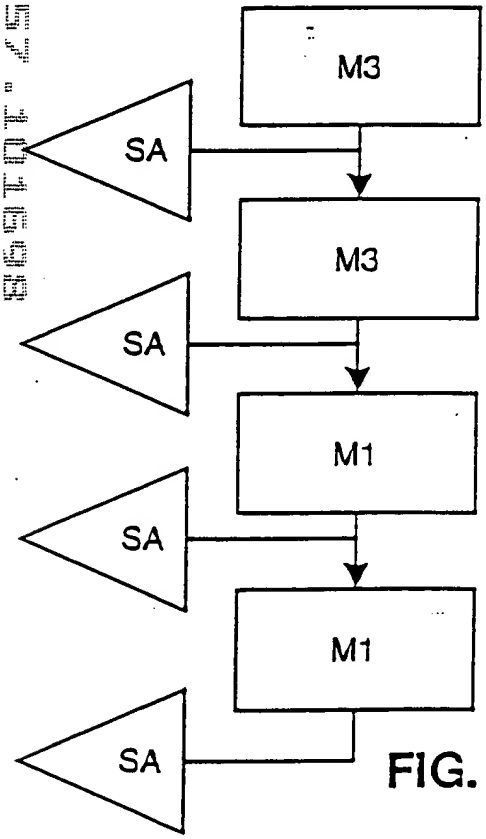


FIG. 16C

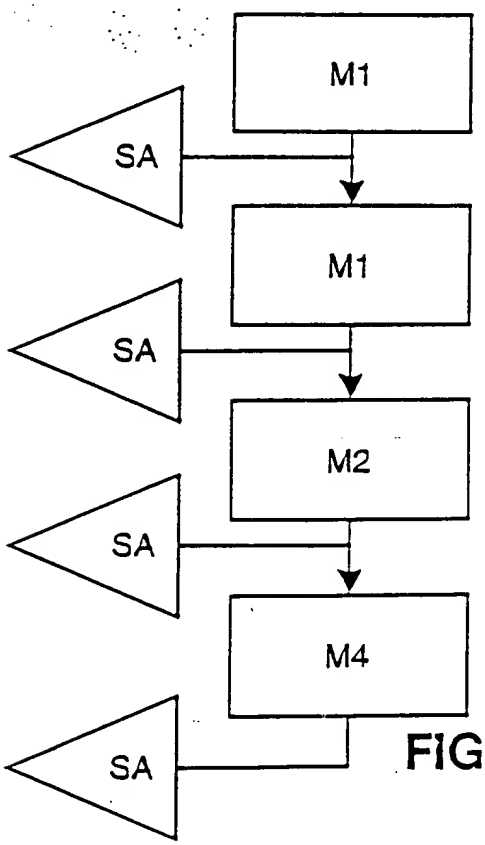


FIG. 16D

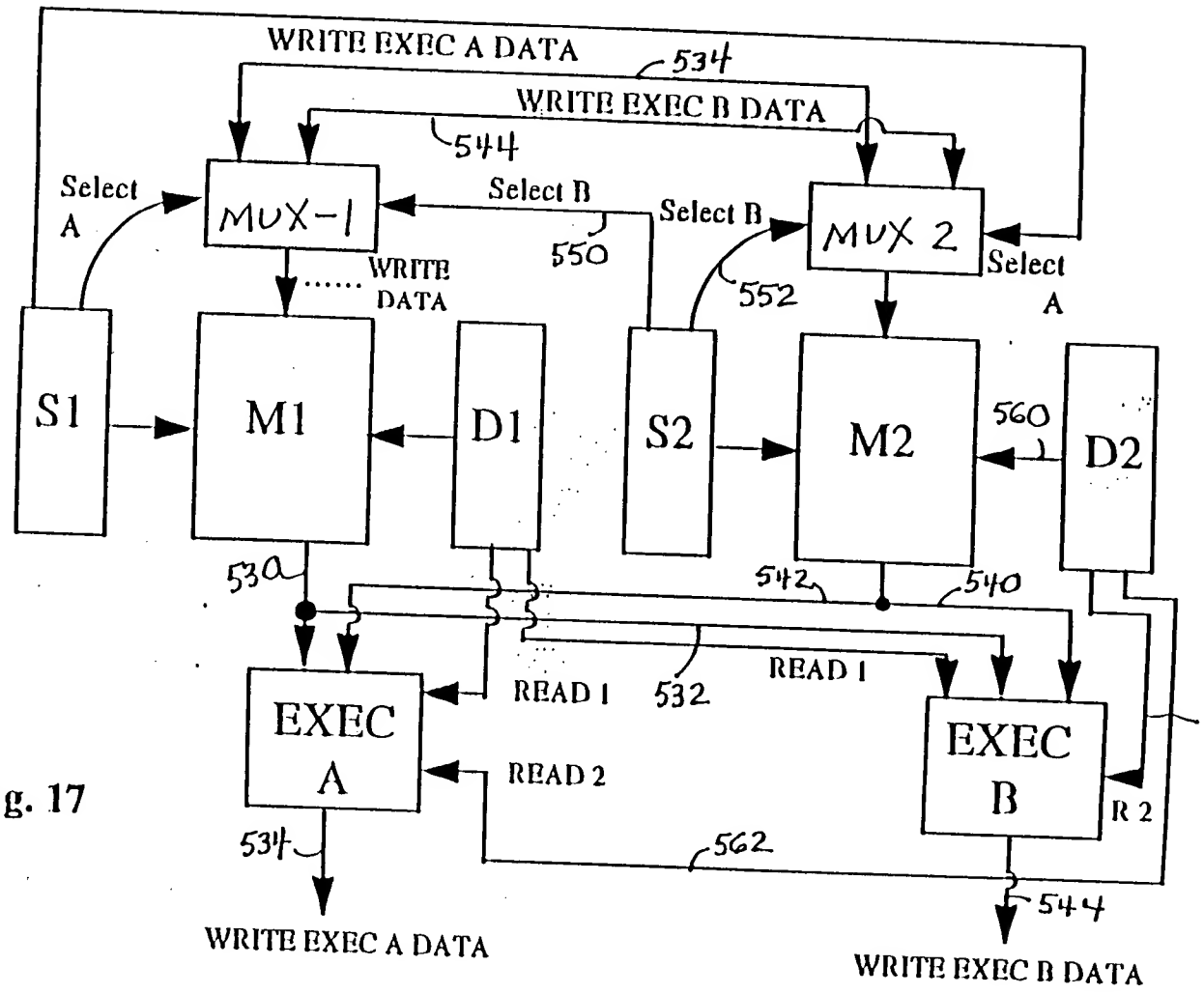


Fig. 17

Note:

Selection Tables in S1, D1, S2, and D2 contain read/write configurations

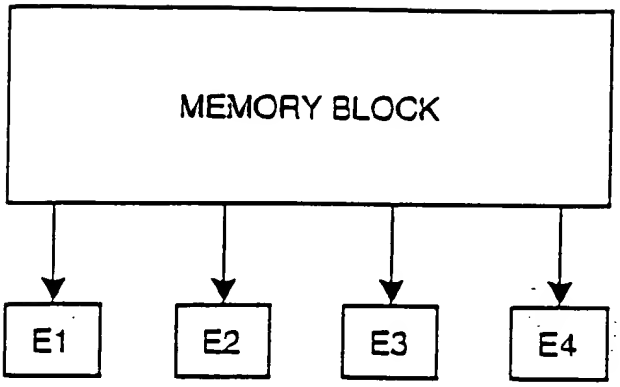


FIG. 18A

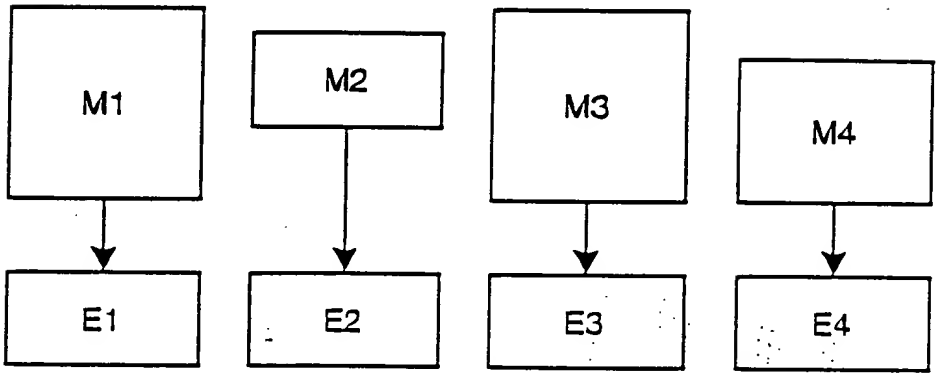


FIG. 18B

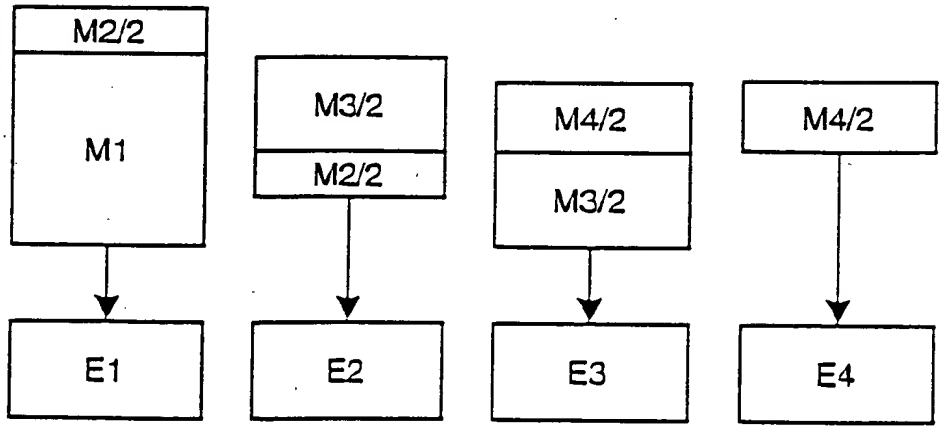


FIG. 18C

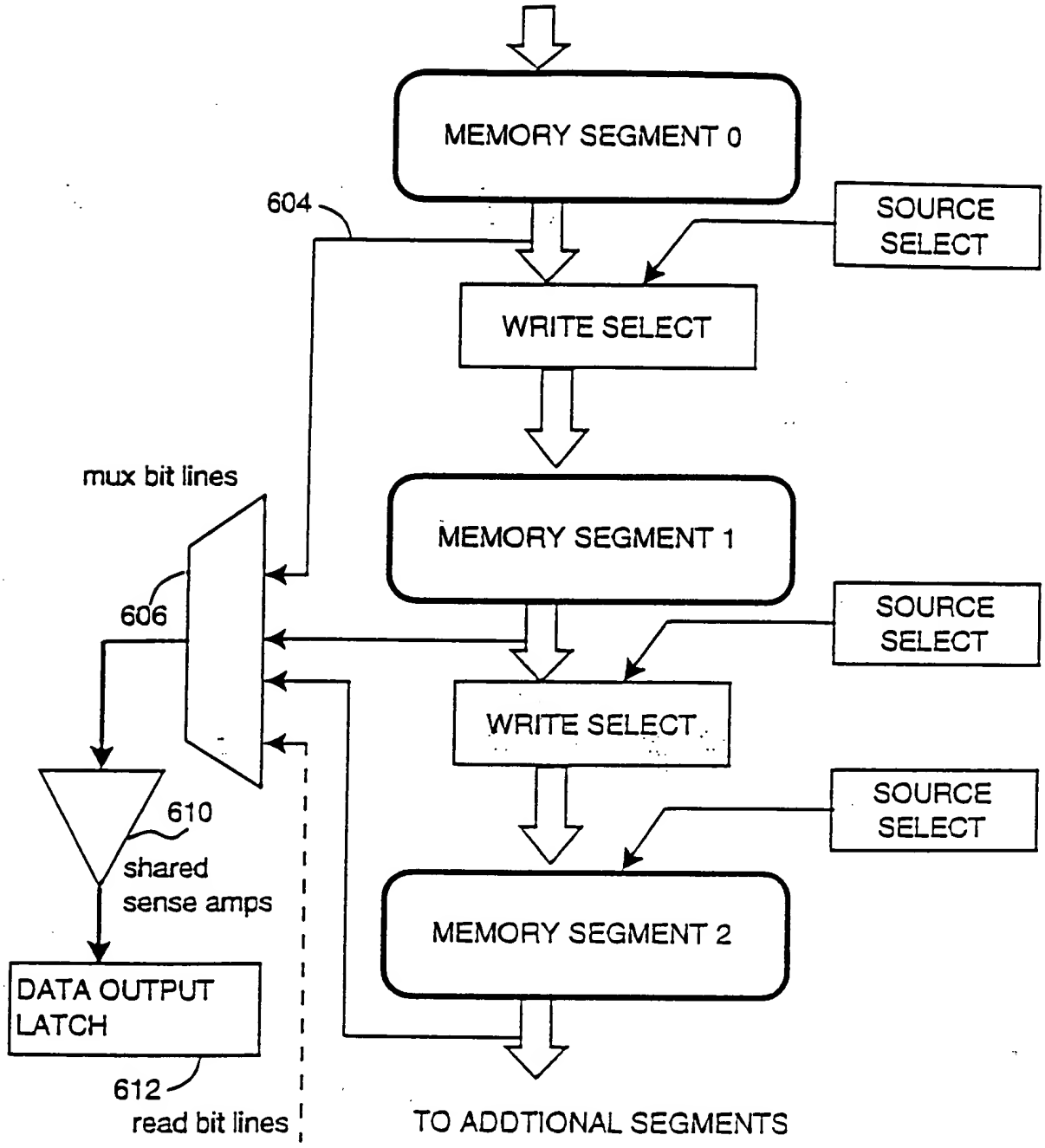

MEMORY SEGMENT 0
604
SOURCE SELECT
WRITE SELECT
mux bit lines
MEMORY SEGMENT 1
606
SOURCE SELECT
WRITE SELECT
SOURCE SELECT
610
shared sense amps
MEMORY SEGMENT 2
DATA OUTPUT LATCH
612
read bit lines
TO ADDTIONAL SEGMENTS

FIG. 19

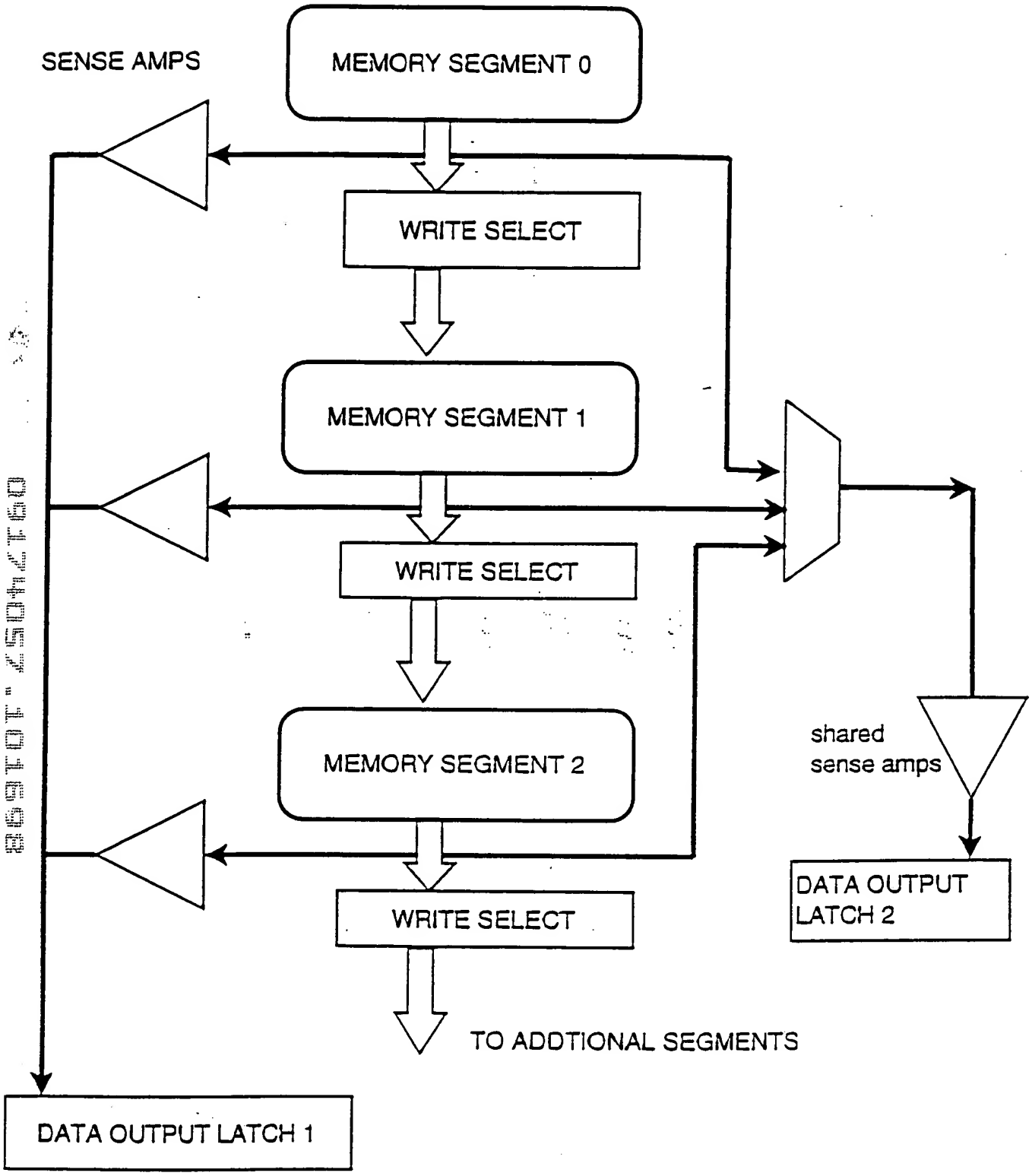

SENSE AMPS
MEMORY SEGMENT 0
WRITE SELECT
MEMORY SEGMENT 1
WRITE SELECT
MEMORY SEGMENT 2
WRITE SELECT
shared
sense amps
DATA OUTPUT
LATCH 2
TO ADDTIONAL SEGMENTS
DATA OUTPUT LATCH 1

FIG. 20

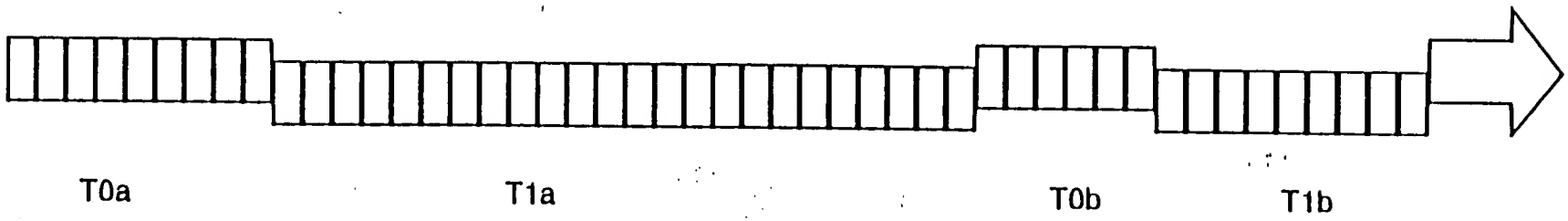


FIG. 21

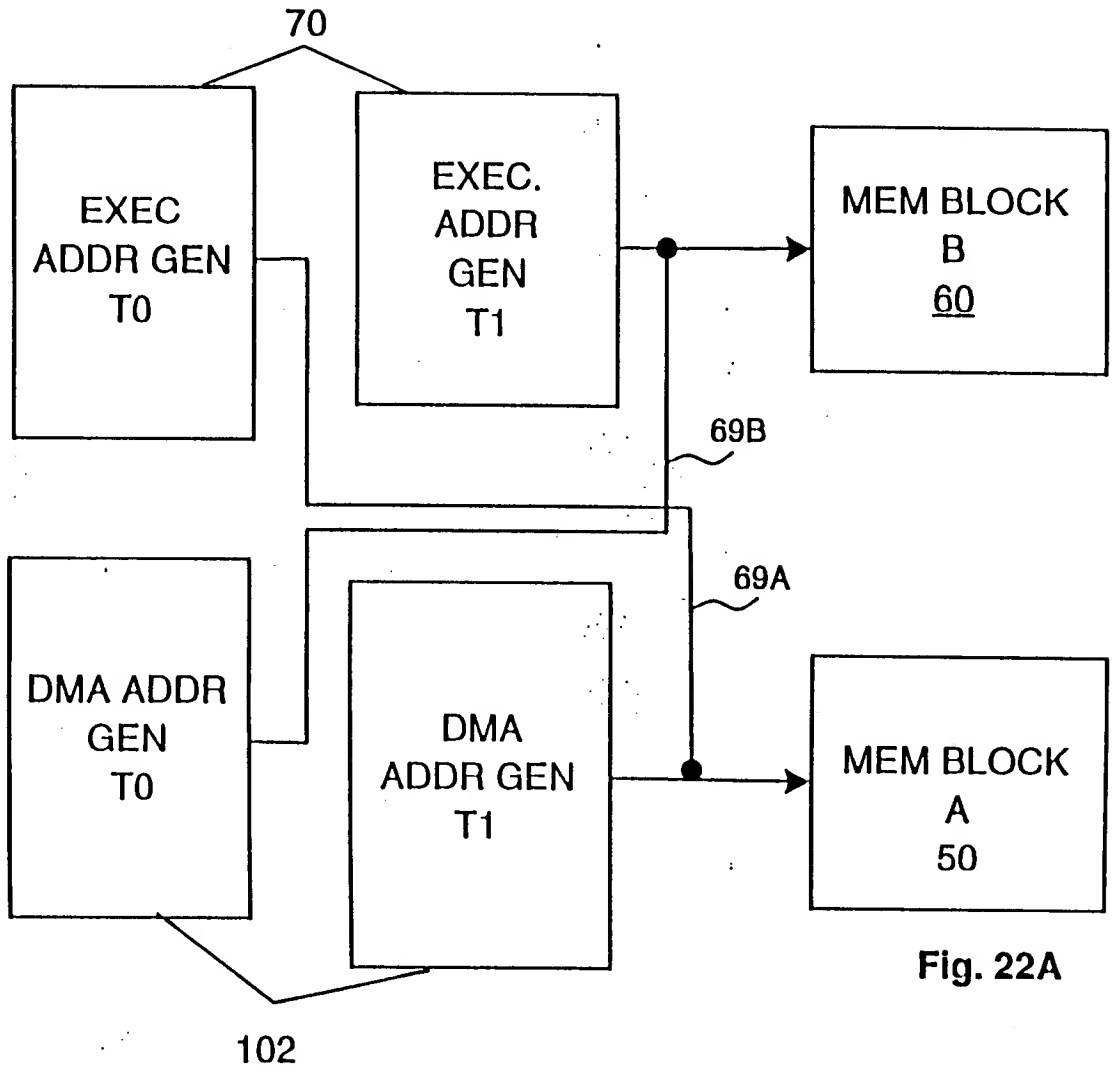


Fig. 22A

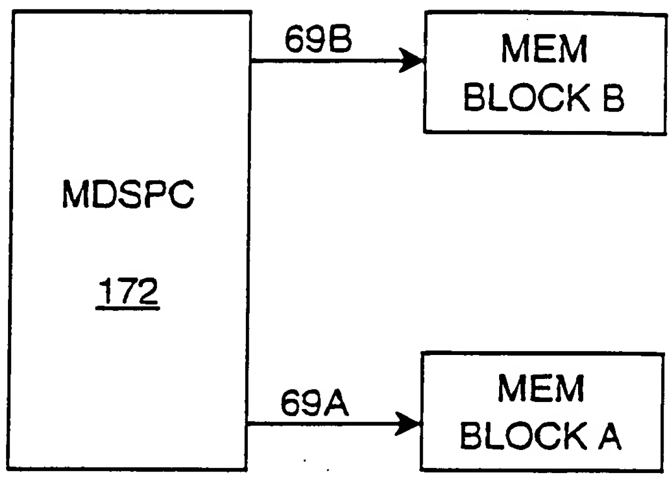


FIG. 22B

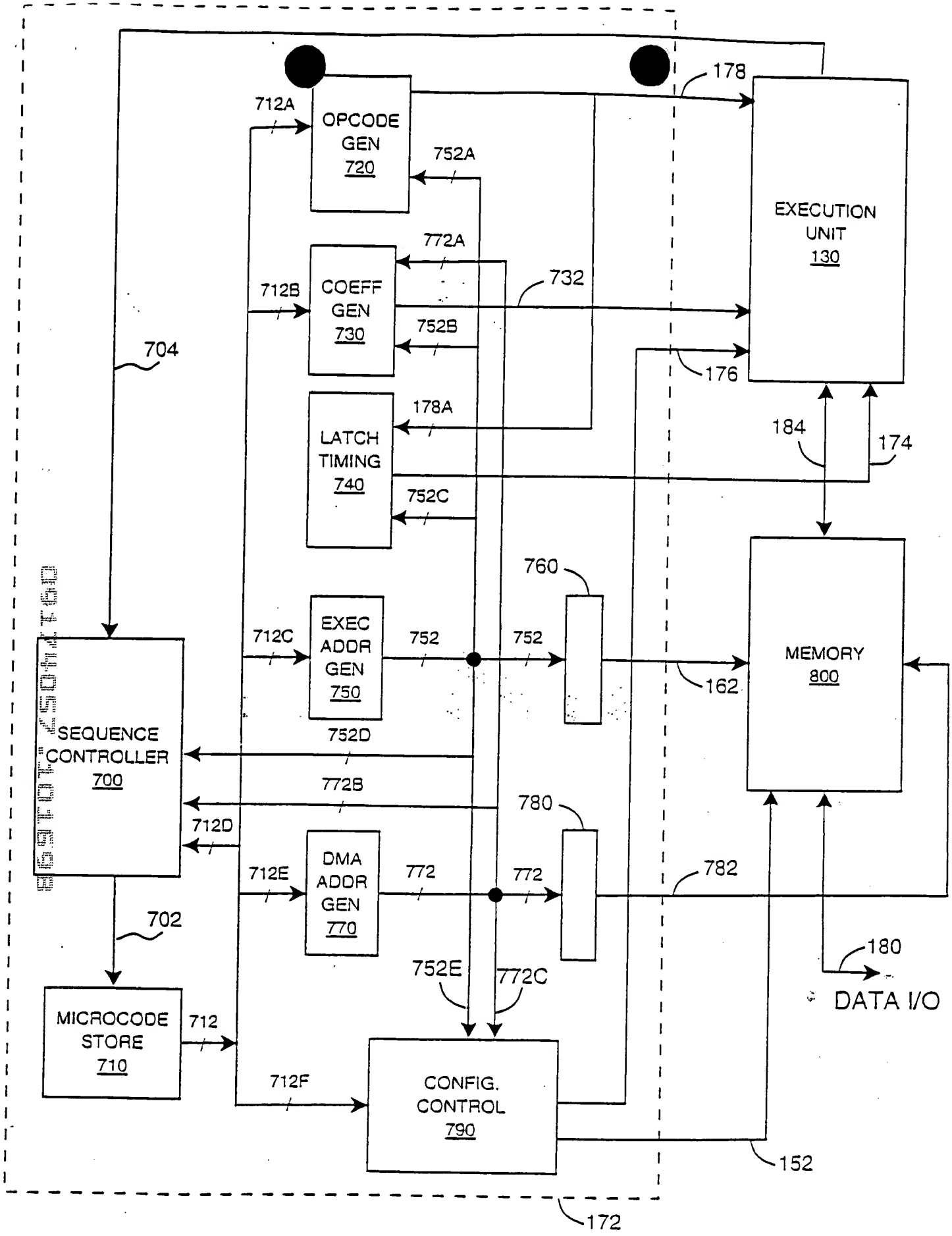

SEQUENCE CONTROLLER 700
MICROCODE STORE 710
OPCODE GEN 720
COEFF GEN 730
LATCH TIMING 740
EXEC ADDR GEN 750
DMA ADDR GEN 770
CONFIG. CONTROL 790
EXECUTION UNIT 130
MEMORY 800
DATA I/O
712A
712B
712C
712D
712E
712F
712
752A
752B
752C
752D
752E
752
772A
772B
772C
772
732
704
702
178
178A
176
184
174
760
780
782
162
180
152
172

FIG. 23A

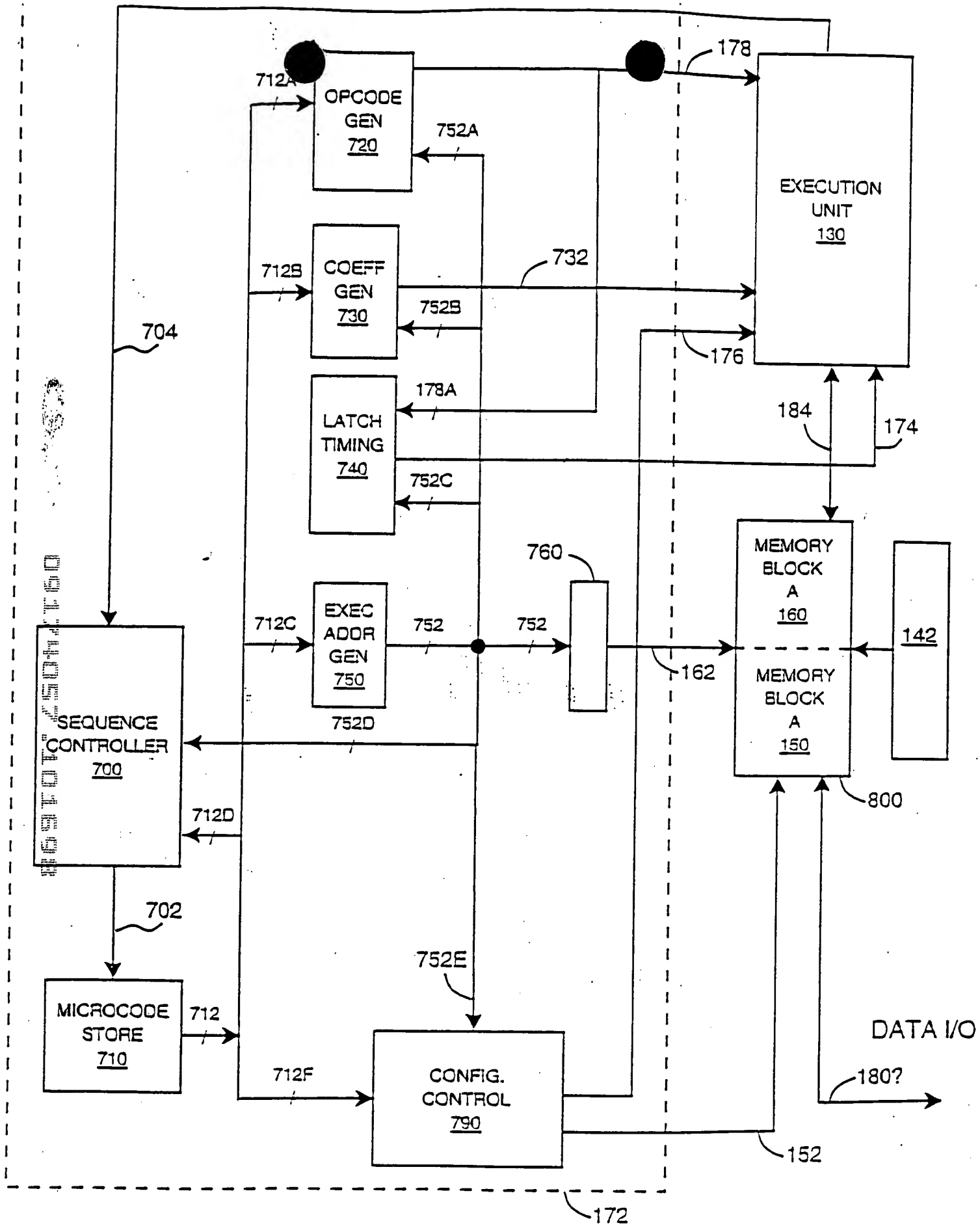

OPCODE GEN 720
712A
752A
178
EXECUTION UNIT 130
COEFF GEN 730
712B
732
752B
704
176
LATCH TIMING 740
178A
184
174
752C
MEMORY BLOCK A 160
760
EXEC ADDR GEN 750
712C
752
752
142
162
MEMORY BLOCK A 150
SEQUENCE CONTROLLER 700
752D
800
712D
702
752E
MICROCODE STORE 710
712
DATA I/O
712F
CONFIG. CONTROL 790
180?
152
172

FIG. 23B

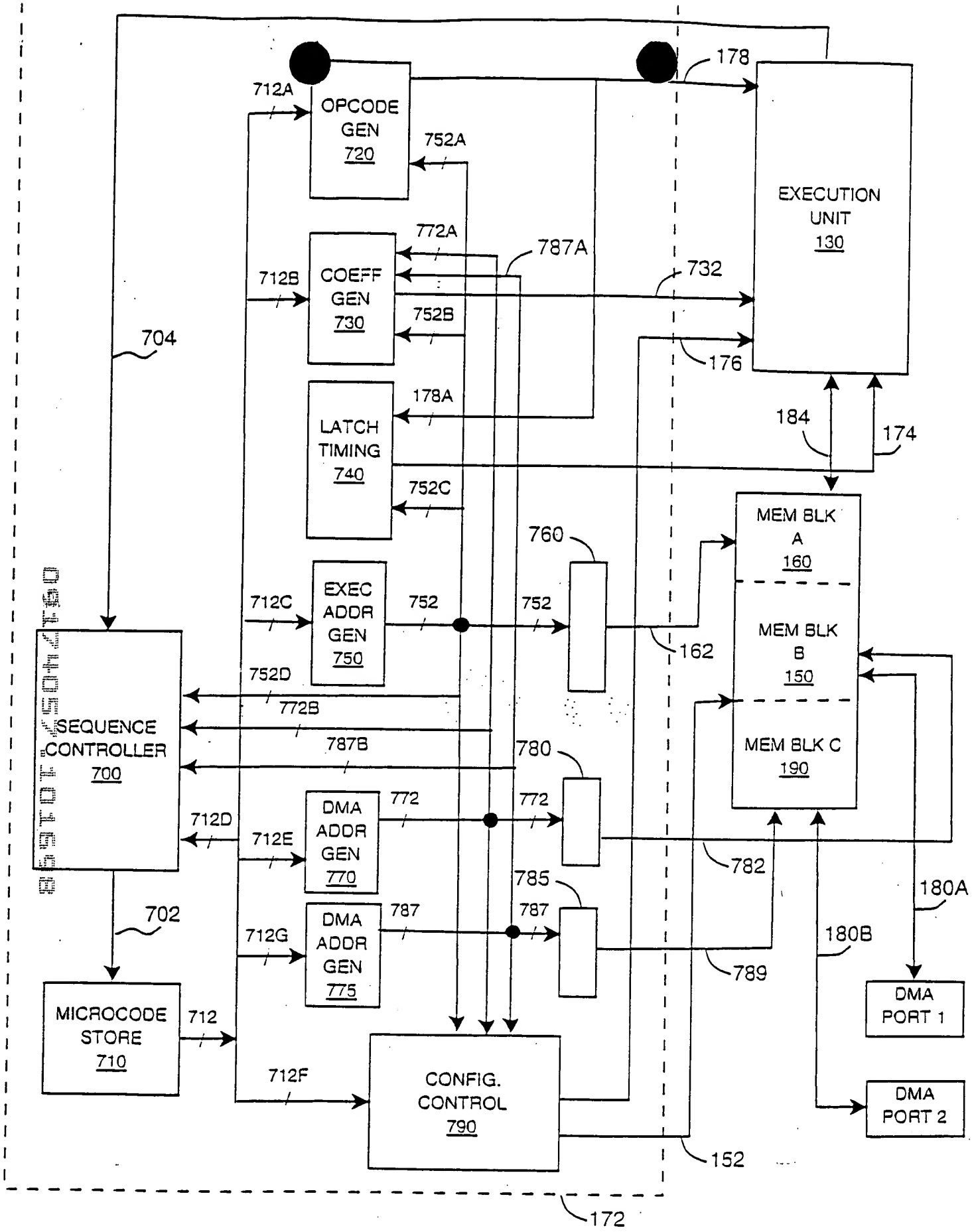

178
712A
OPCODE GEN 720
752A
EXECUTION UNIT 130
772A
787A
712B
COEFF GEN 730
732
752B
704
176
178A
LATCH TIMING 740
184
174
752C
MEM BLK A 160
760
712C
EXEC ADDR GEN 750
752
752
MEM BLK B 150
162
752D
772B
SEQUENCE CONTROLLER 700
787B
780
MEM BLK C 190
772
772
712D
712E
DMA ADDR GEN 770
782
785
180A
787
787
712G
DMA ADDR GEN 775
180B
789
702
MICROCODE STORE 710
712
DMA PORT 1
712F
CONFIG. CONTROL 790
DMA PORT 2
152
172

FIG. 23C

RESS	FUNCTION
0x710	FFT RADIX 2
0x905	FIR FILTER
0x2100	CONVOLUTION

FIG. 24A

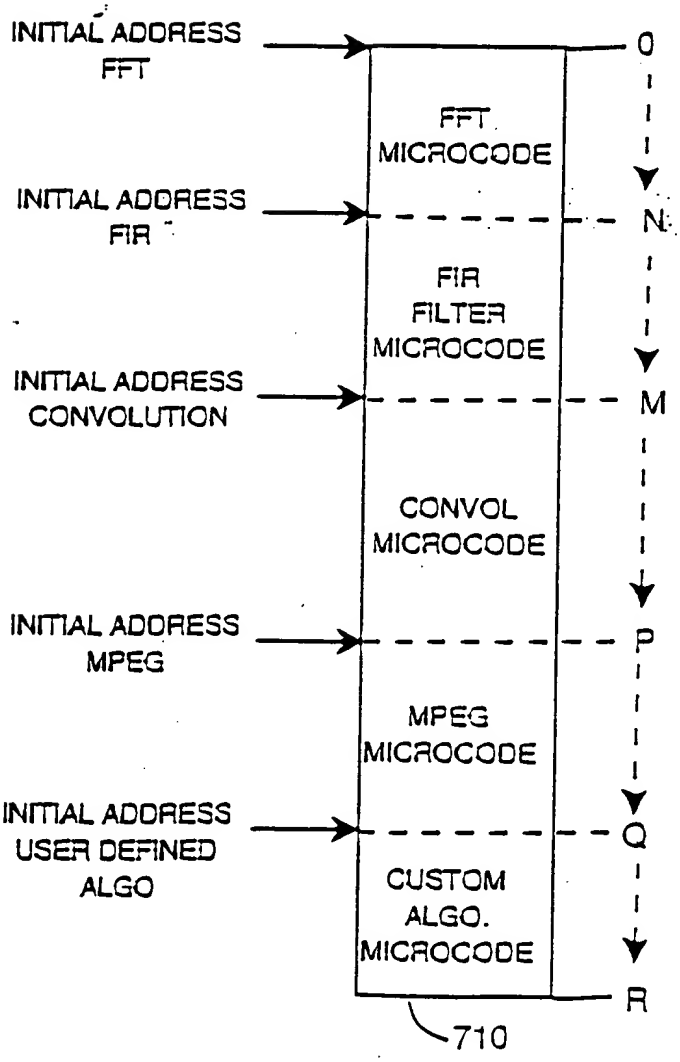


FIG. 24B

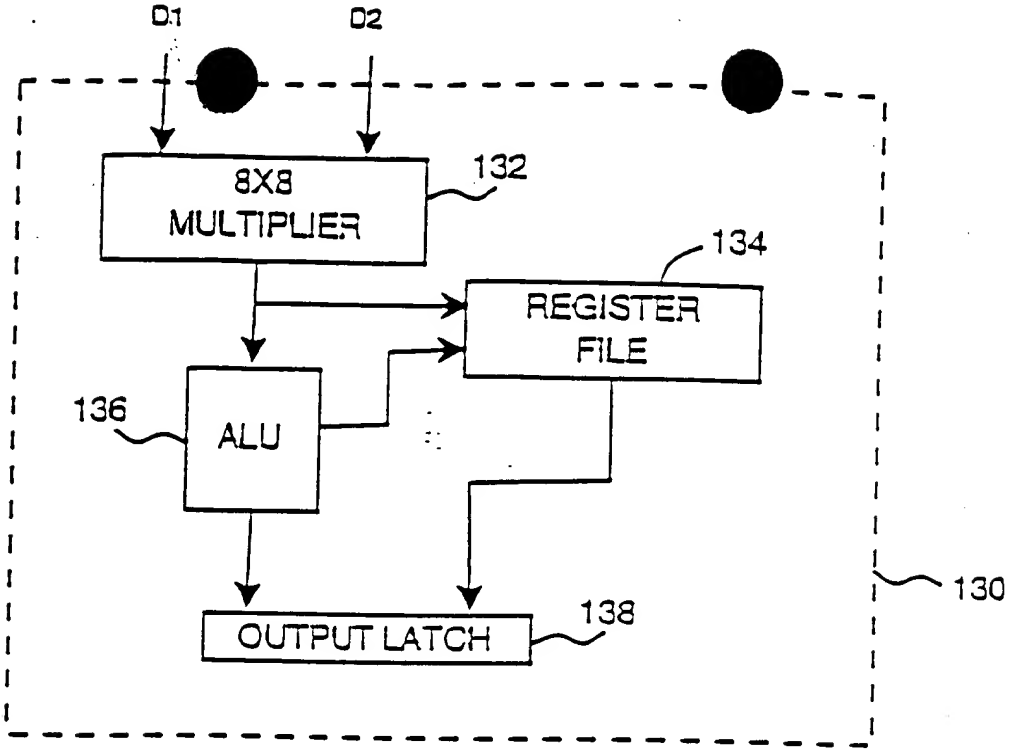

D1
D2
8X8
MULTIPLIER
132
134
REGISTER
FILE
136
ALU
130
OUTPUT LATCH
138

FIG. 25

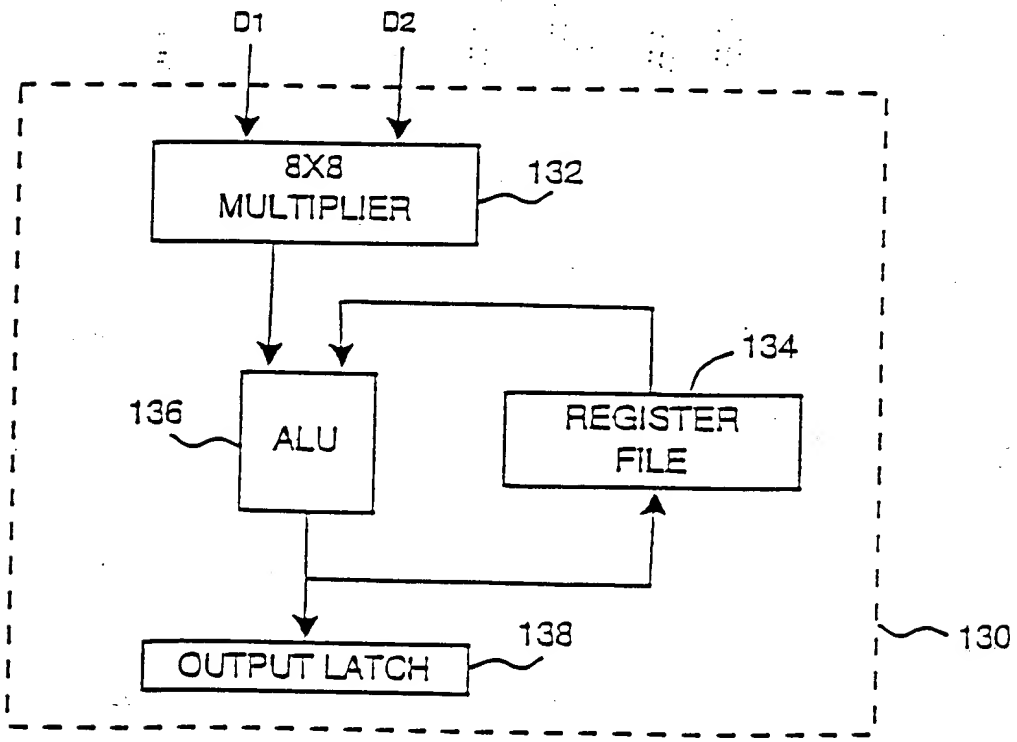

D1
D2
8X8
MULTIPLIER
132
134
136
ALU
REGISTER
FILE
130
OUTPUT LATCH
138

FIG. 26

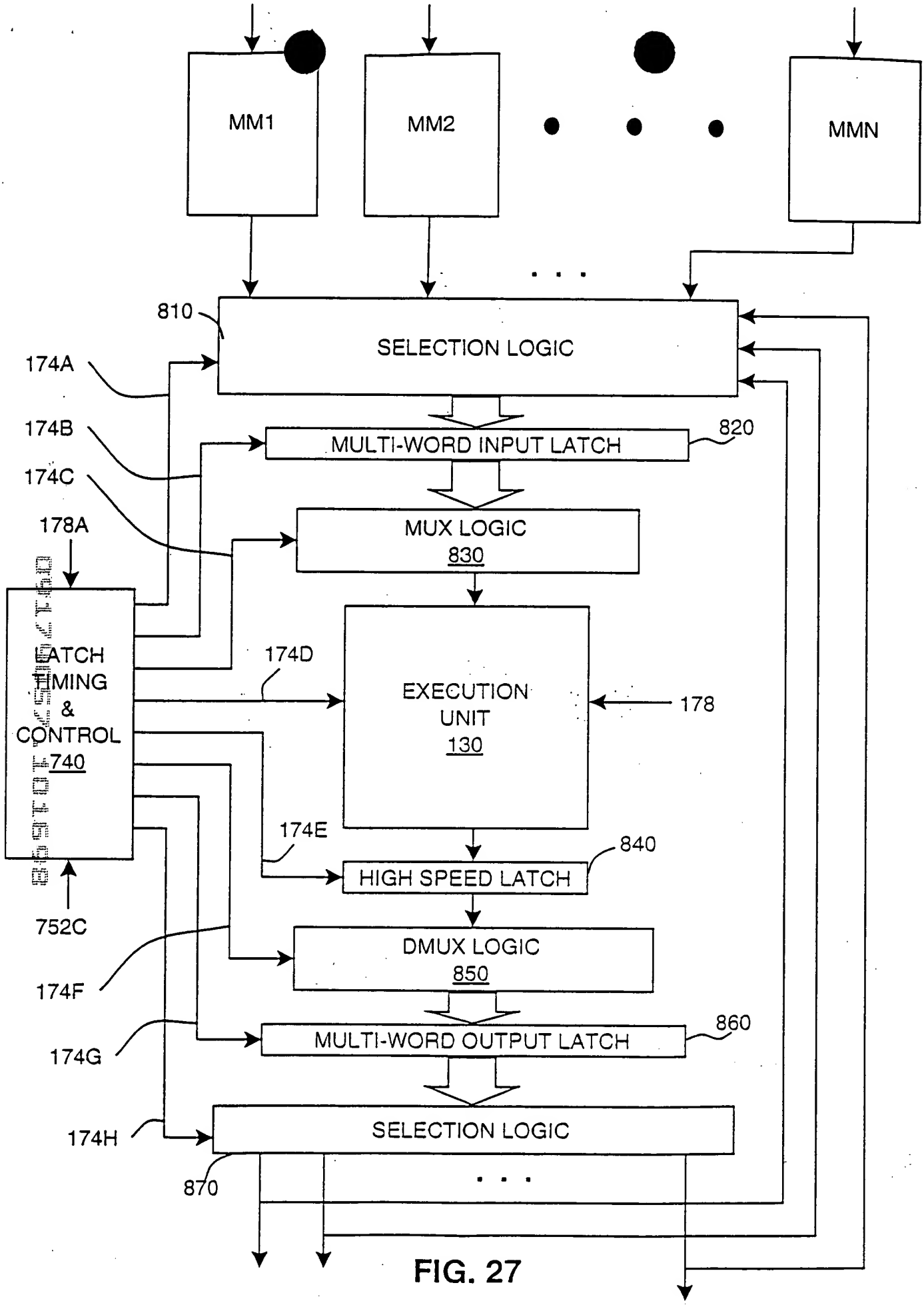

MM1
MM2
MMN
810
SELECTION LOGIC
174A
174B
174C
178A
MULTI-WORD INPUT LATCH
820
MUX LOGIC
830
LATCH TIMING & CONTROL
740
174D
EXECUTION UNIT
130
178
174E
840
HIGH SPEED LATCH
752C
DMUX LOGIC
850
174F
174G
MULTI-WORD OUTPUT LATCH
860
174H
SELECTION LOGIC
870

FIG. 27

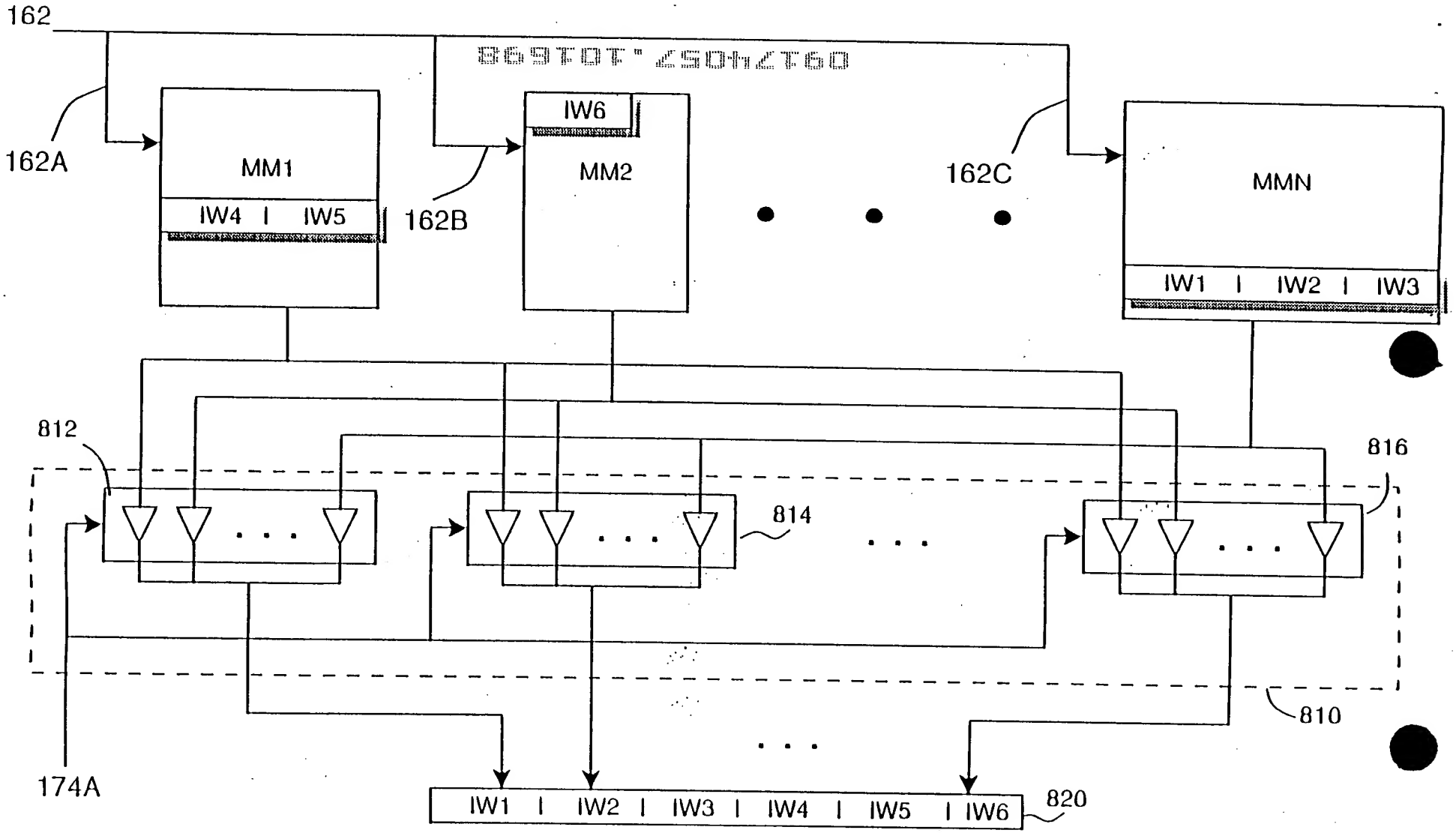

162
162A
MM1
IW4 I IW5
162B
IW6
MM2
162C
MMN
IW1 I IW2 I IW3
812
816
814
810
174A
IW1 I IW2 I IW3 I IW4 I IW5 I IW6
820

FIG. 28

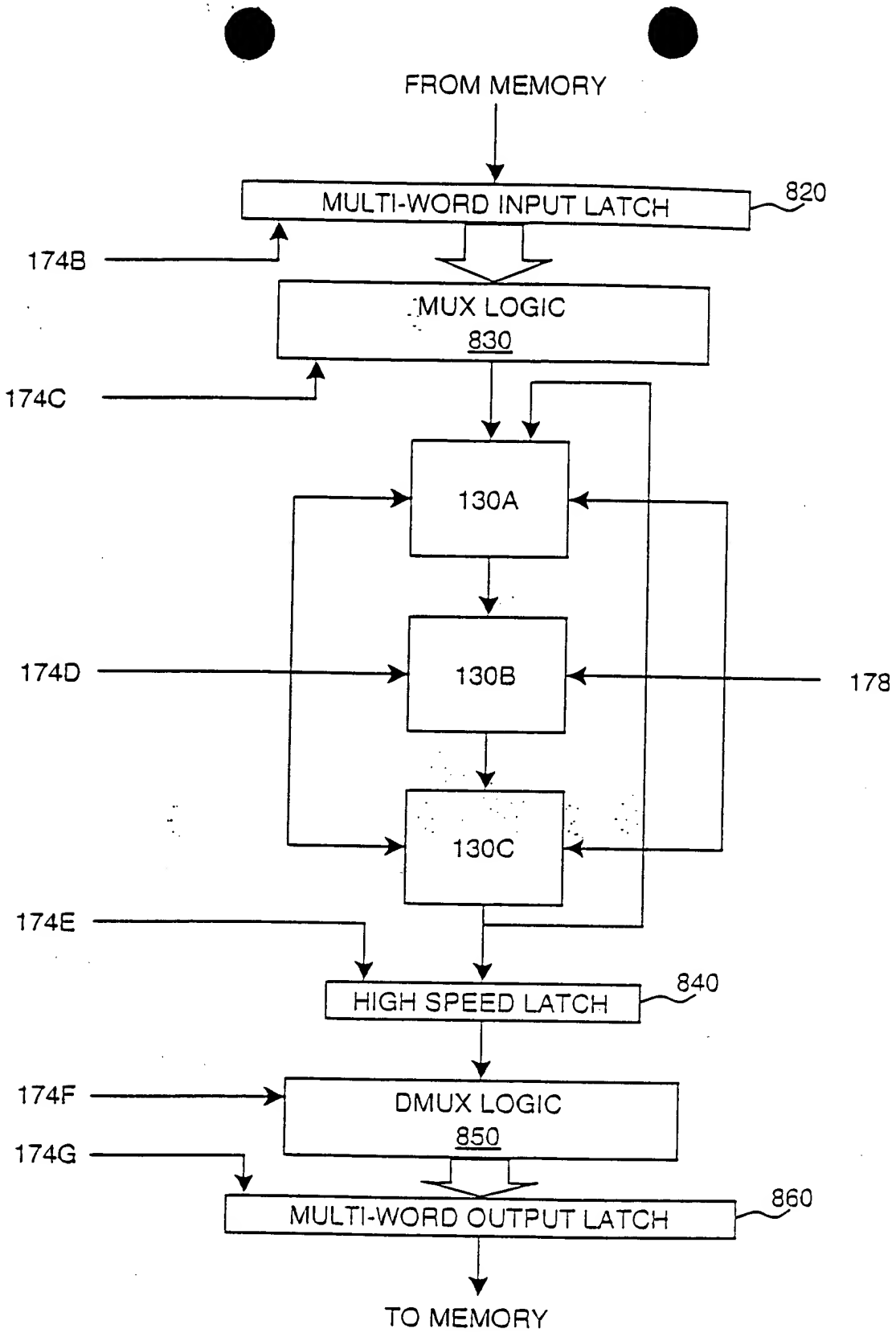

FROM MEMORY
MULTI-WORD INPUT LATCH
820
174B
MUX LOGIC
830
174C
130A
130B
174D
178
130C
174E
HIGH SPEED LATCH
840
174F
DMUX LOGIC
850
174G
MULTI-WORD OUTPUT LATCH
860
TO MEMORY

FIG. 29

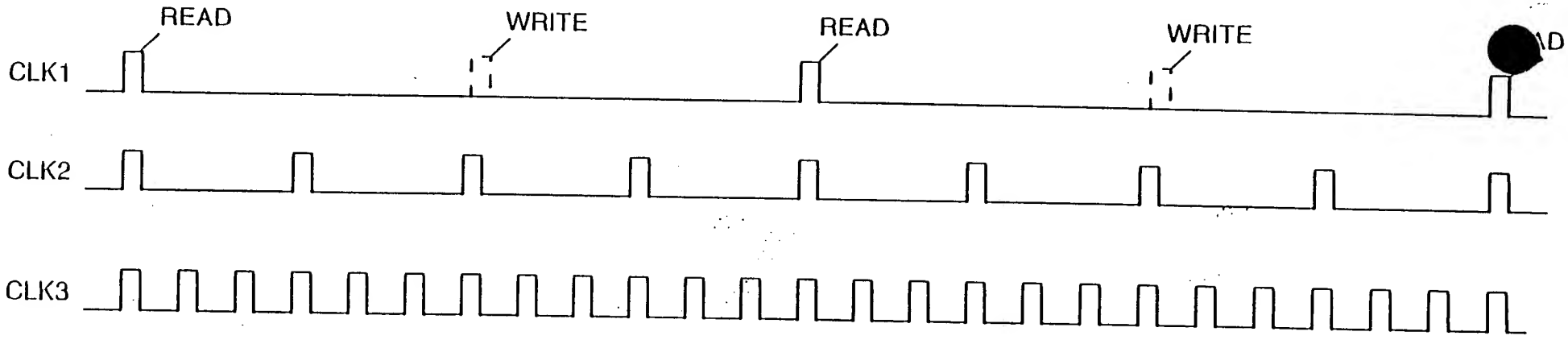


FIG. 30A

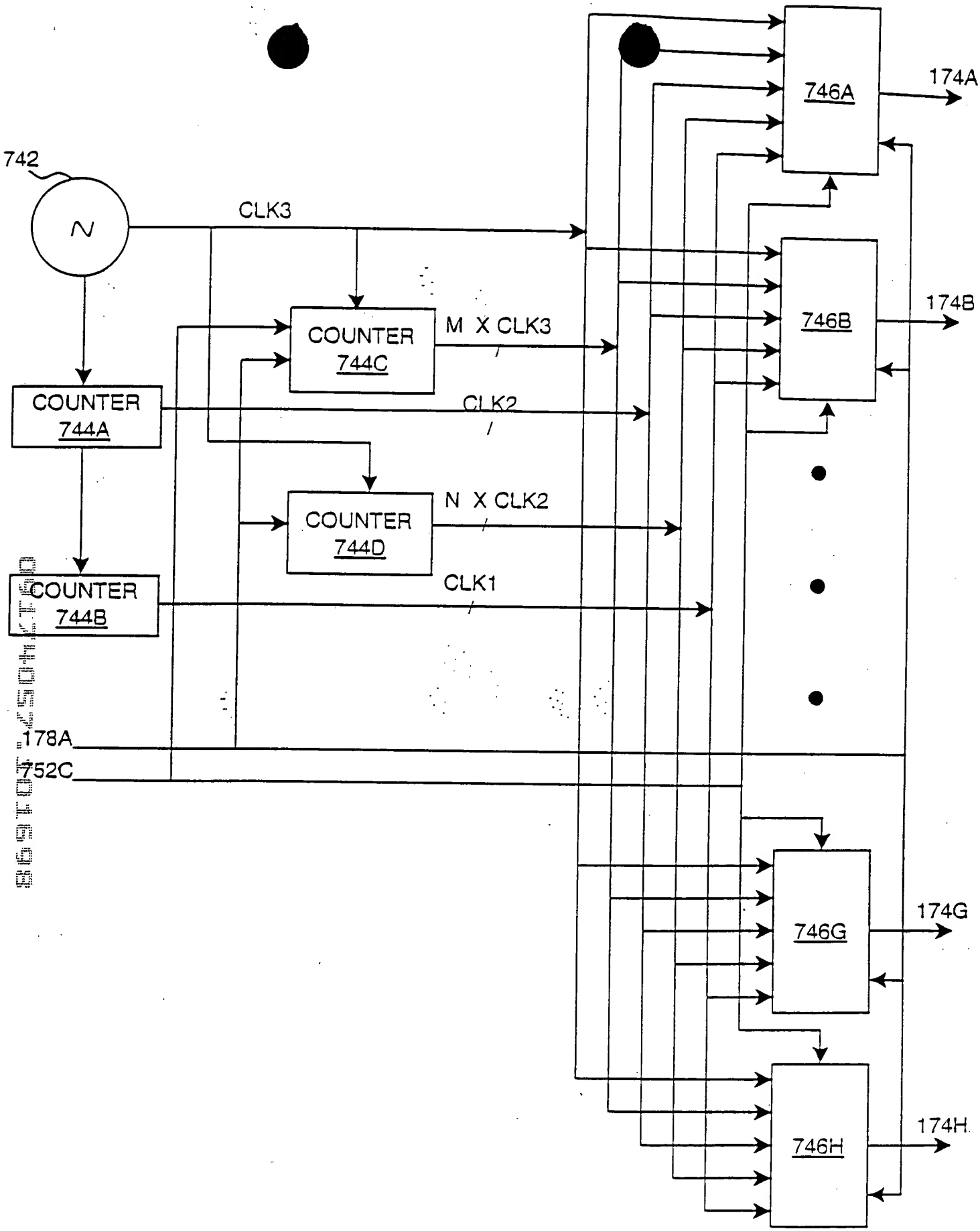

742
N
CLK3
COUNTER 744A
COUNTER 744B
COUNTER 744C
M X CLK3
CLK2
COUNTER 744D
N X CLK2
CLK1
178A
752C
746A
174A
746B
174B
746G
174G
746H
174H

FIG. 30B

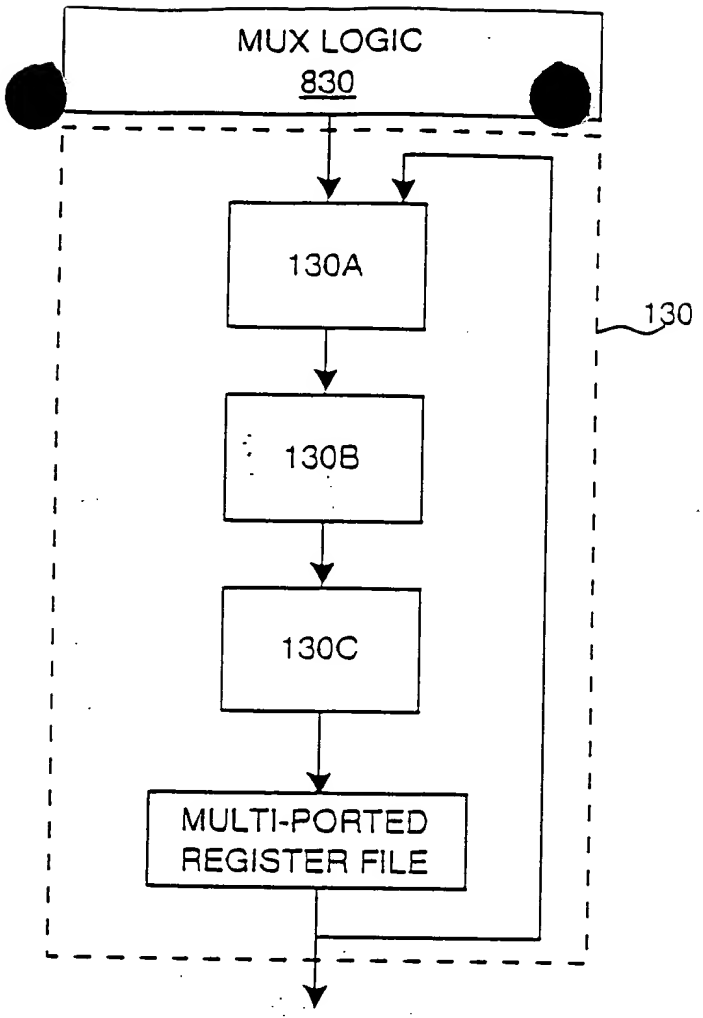


FIG. 31

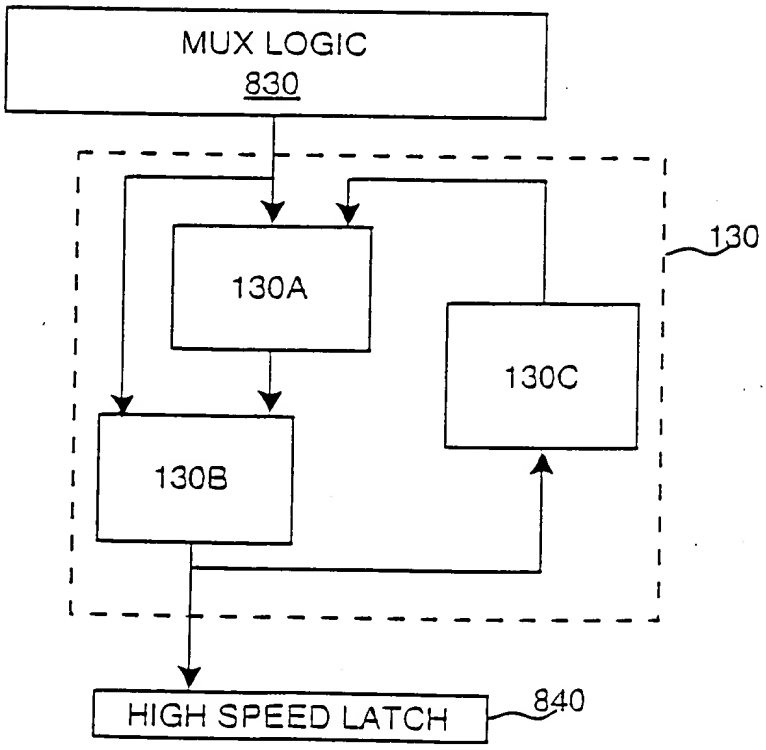


FIG. 32

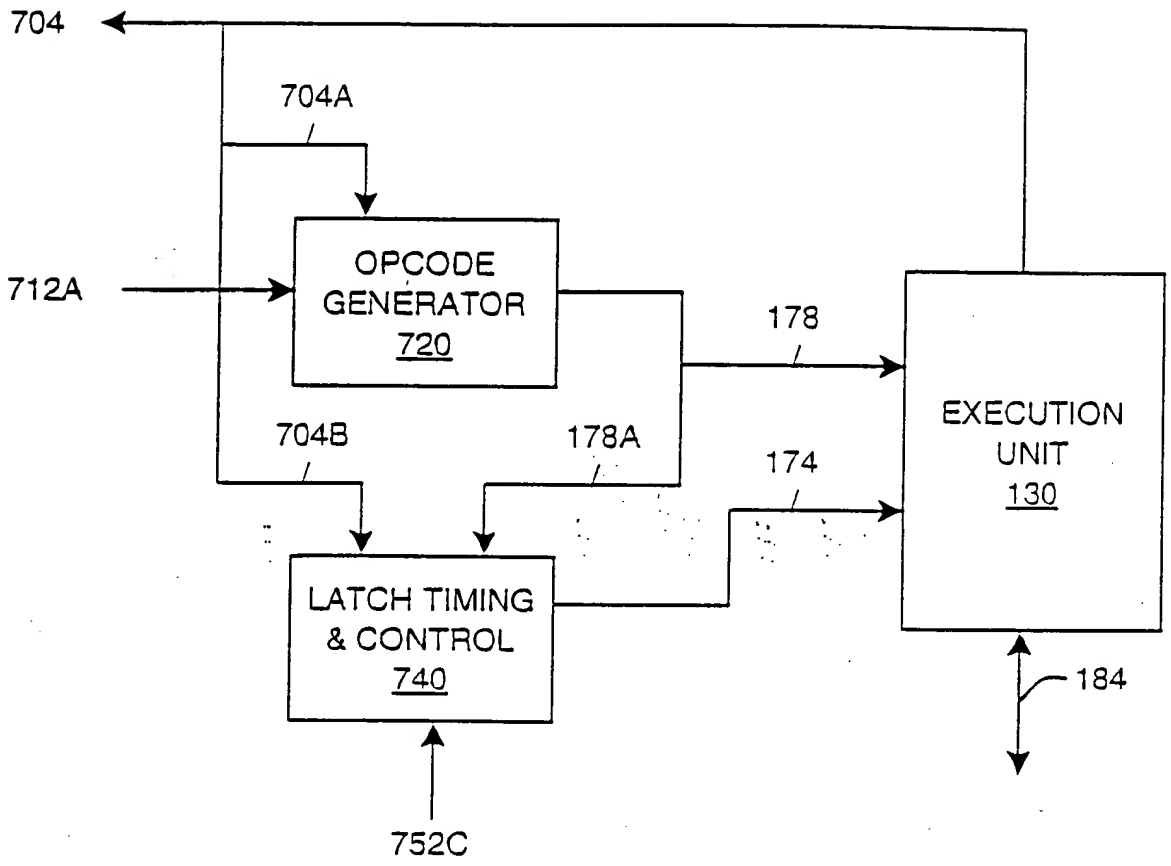

704
704A
712A
OPCODE
GENERATOR
720
178
EXECUTION
UNIT
130
704B
178A
174
LATCH TIMING
& CONTROL
740
184
752C

FIG. 33

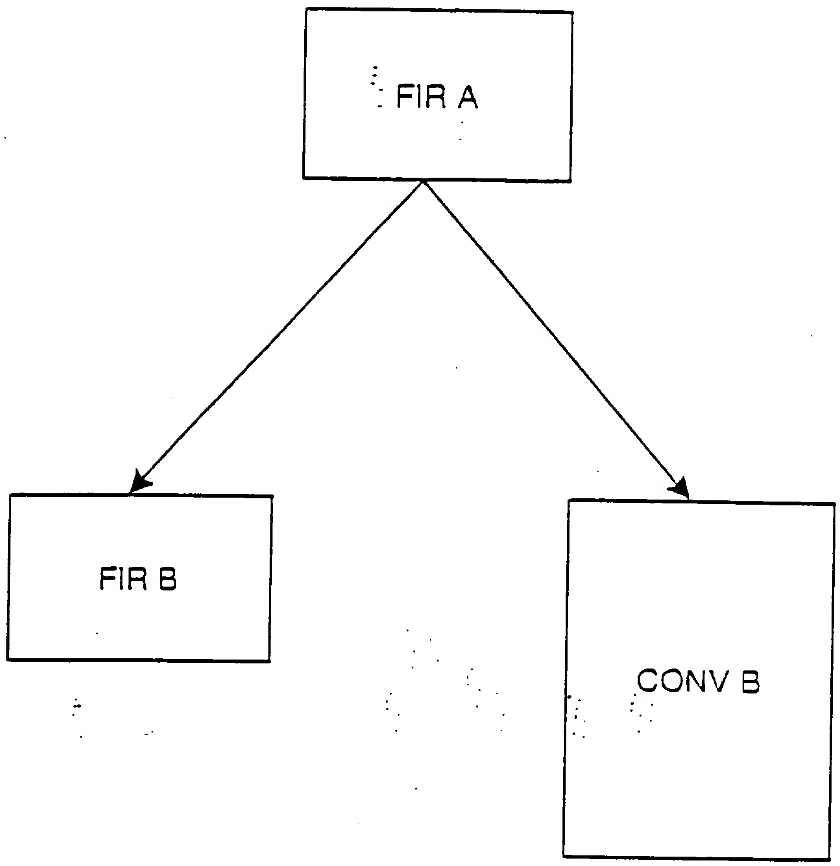


FIG. 34

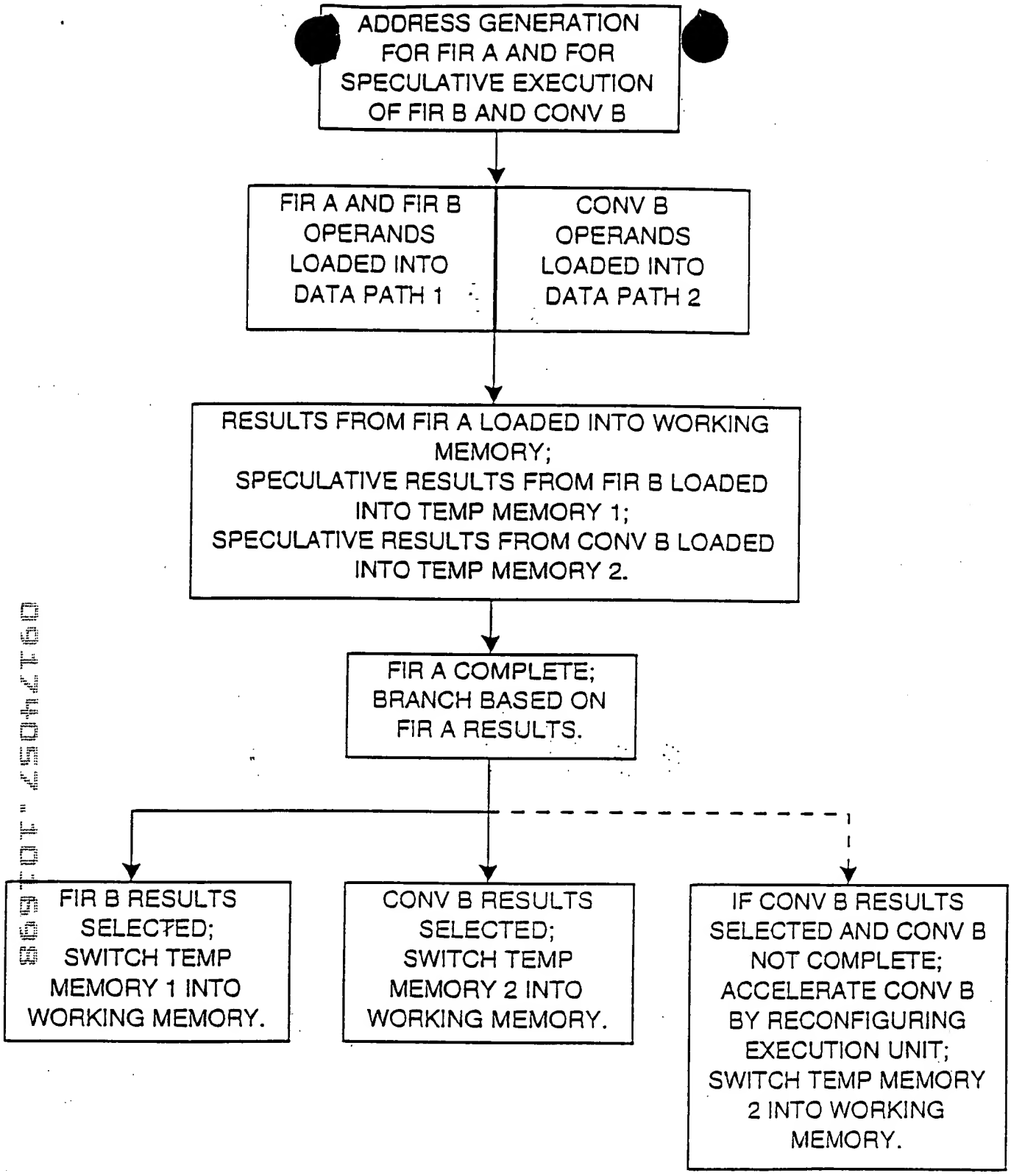

ADDRESS GENERATION FOR FIR A AND FOR SPECULATIVE EXECUTION OF FIR B AND CONV B
FIR A AND FIR B OPERANDS LOADED INTO DATA PATH 1
CONV B OPERANDS LOADED INTO DATA PATH 2
RESULTS FROM FIR A LOADED INTO WORKING MEMORY; SPECULATIVE RESULTS FROM FIR B LOADED INTO TEMP MEMORY 1; SPECULATIVE RESULTS FROM CONV B LOADED INTO TEMP MEMORY 2.
FIR A COMPLETE; BRANCH BASED ON FIR A RESULTS.
FIR B RESULTS SELECTED; SWITCH TEMP MEMORY 1 INTO WORKING MEMORY.
CONV B RESULTS SELECTED; SWITCH TEMP MEMORY 2 INTO WORKING MEMORY.
IF CONV B RESULTS SELECTED AND CONV B NOT COMPLETE; ACCELERATE CONV B BY RECONFIGURING EXECUTION UNIT; SWITCH TEMP MEMORY 2 INTO WORKING MEMORY.

FIG. 35

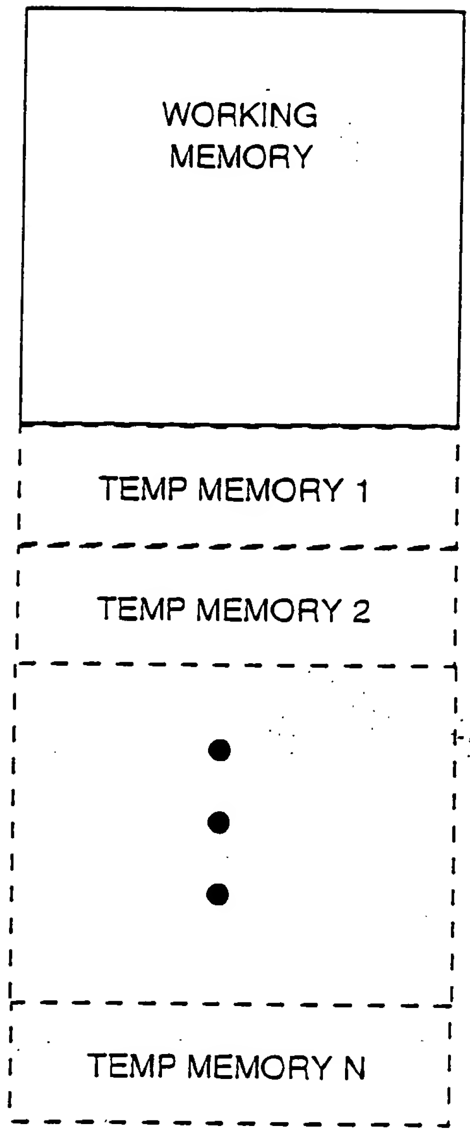
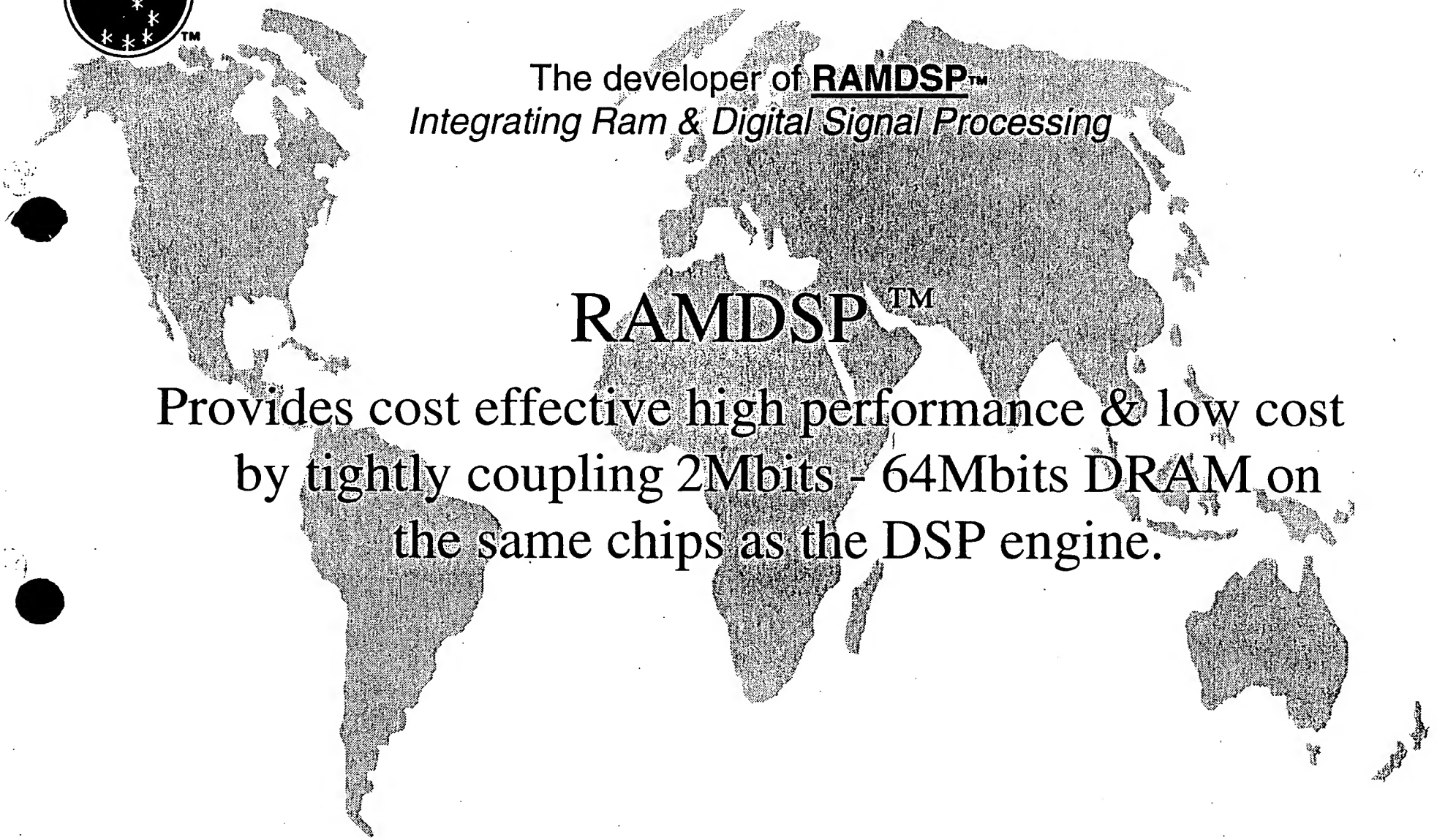


FIG. 36

Stellar Technologies, Ltd.



The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

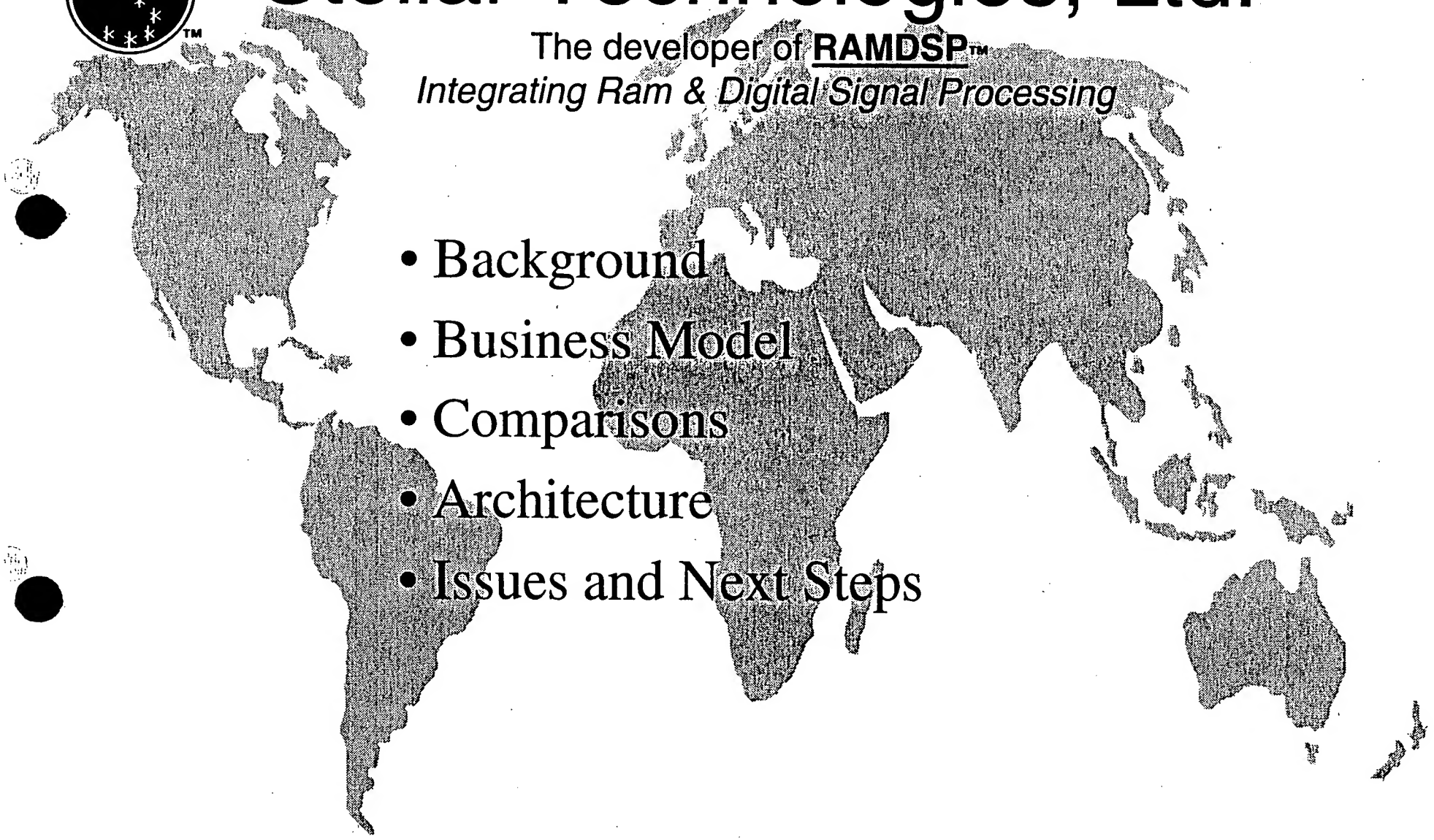
RAMDSP ™

Provides cost effective high performance & low cost by tightly coupling 2Mbits - 64Mbits DRAM on the same chips as the DSP engine.

Stellar Technologies, Ltd.

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

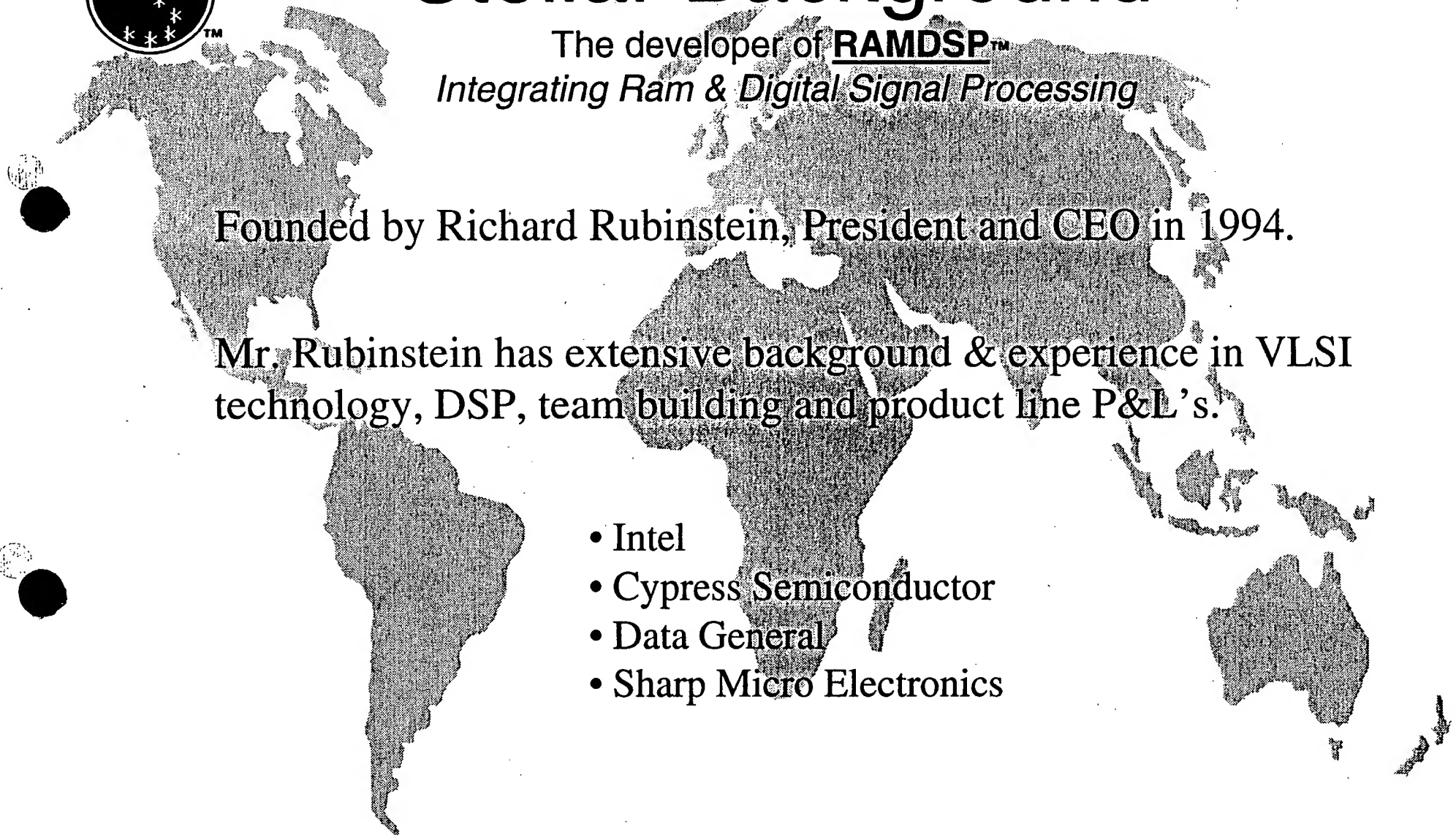


- Background
- Business Model
- Comparisons
- Architecture
- Issues and Next Steps

Stellar Background

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Founded by Richard Rubinstein, President and CEO in 1994.

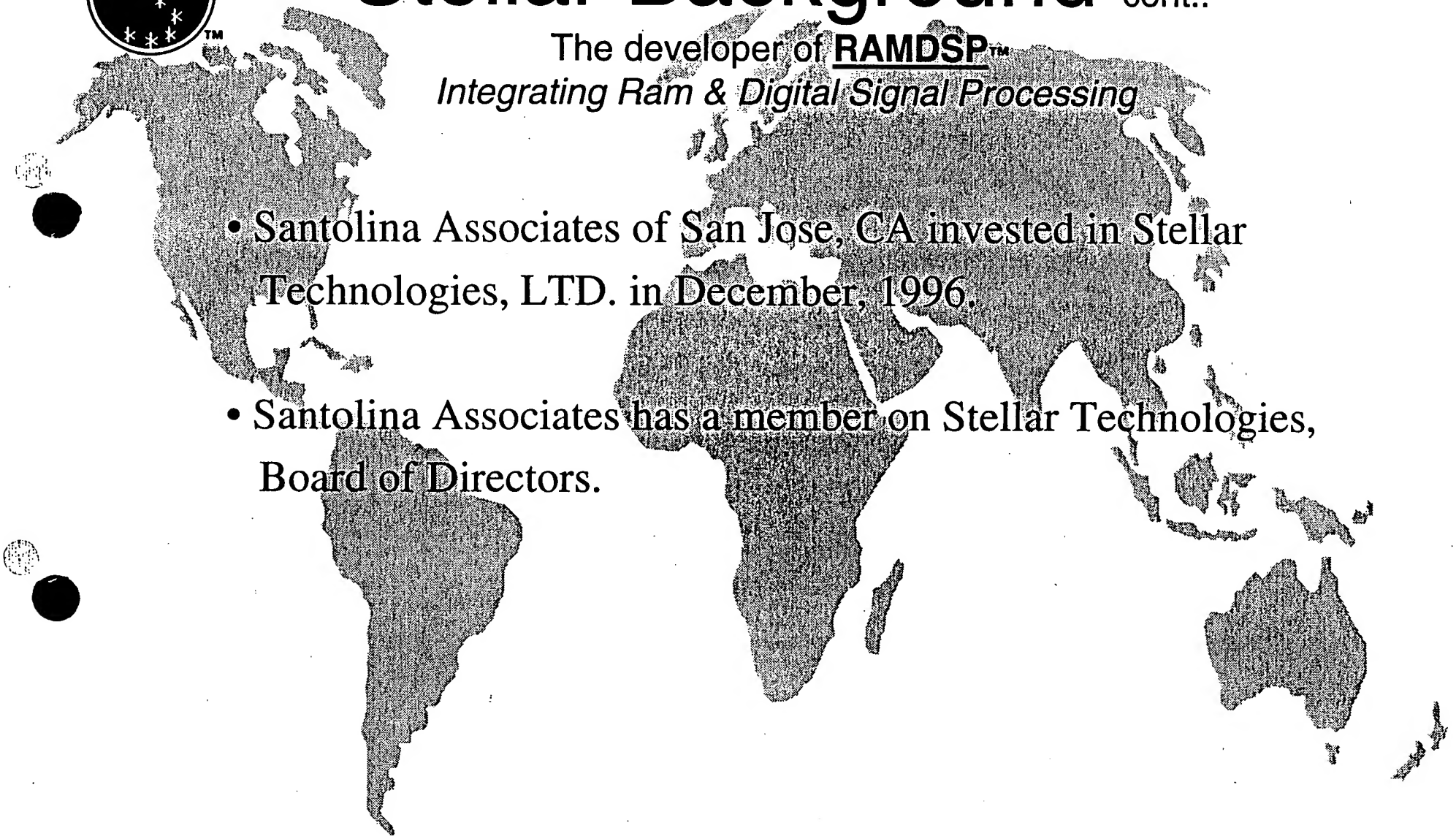
Mr. Rubinstein has extensive background & experience in VLSI technology, DSP, team building and product line P&L's.

- Intel
- Cypress Semiconductor
- Data General
- Sharp Micro Electronics

Stellar Background cont..

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



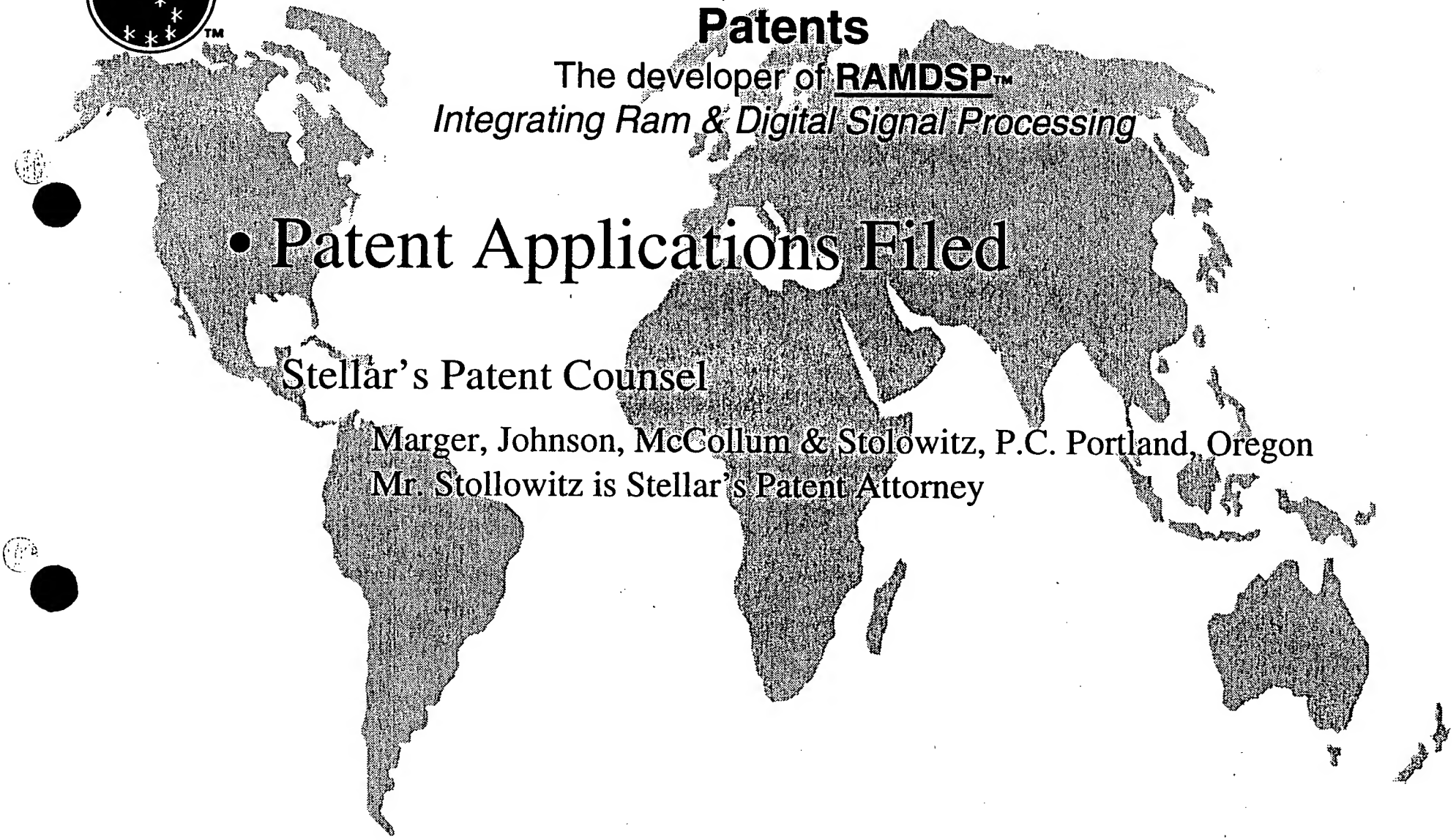
- Santolina Associates of San Jose, CA invested in Stellar Technologies, LTD. in December, 1996.
- Santolina Associates has a member on Stellar Technologies, Board of Directors.

Stellar Background

Patents

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Patent Applications Filed

Stellar's Patent Counsel

Marger, Johnson, McCollum & Stolowitz, P.C. Portland, Oregon

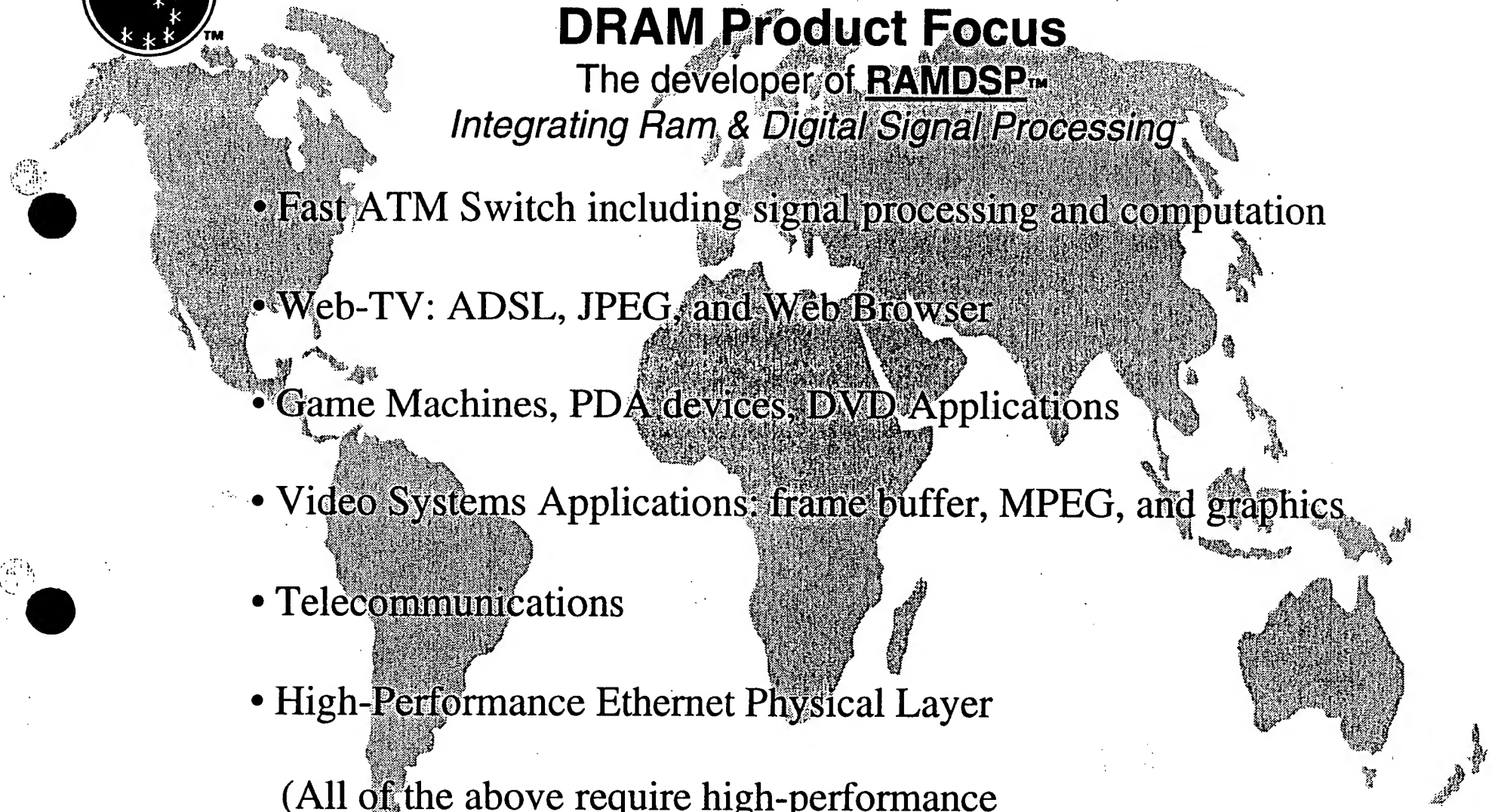
Mr. Stollowitz is Stellar's Patent Attorney

Stellar Business Model

DRAM Product Focus

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Fast ATM Switch including signal processing and computation
- Web-TV: ADSL, JPEG, and Web Browser
- Game Machines, PDA devices, DVD Applications
- Video Systems Applications: frame buffer, MPEG, and graphics
- Telecommunications
- High-Performance Ethernet Physical Layer

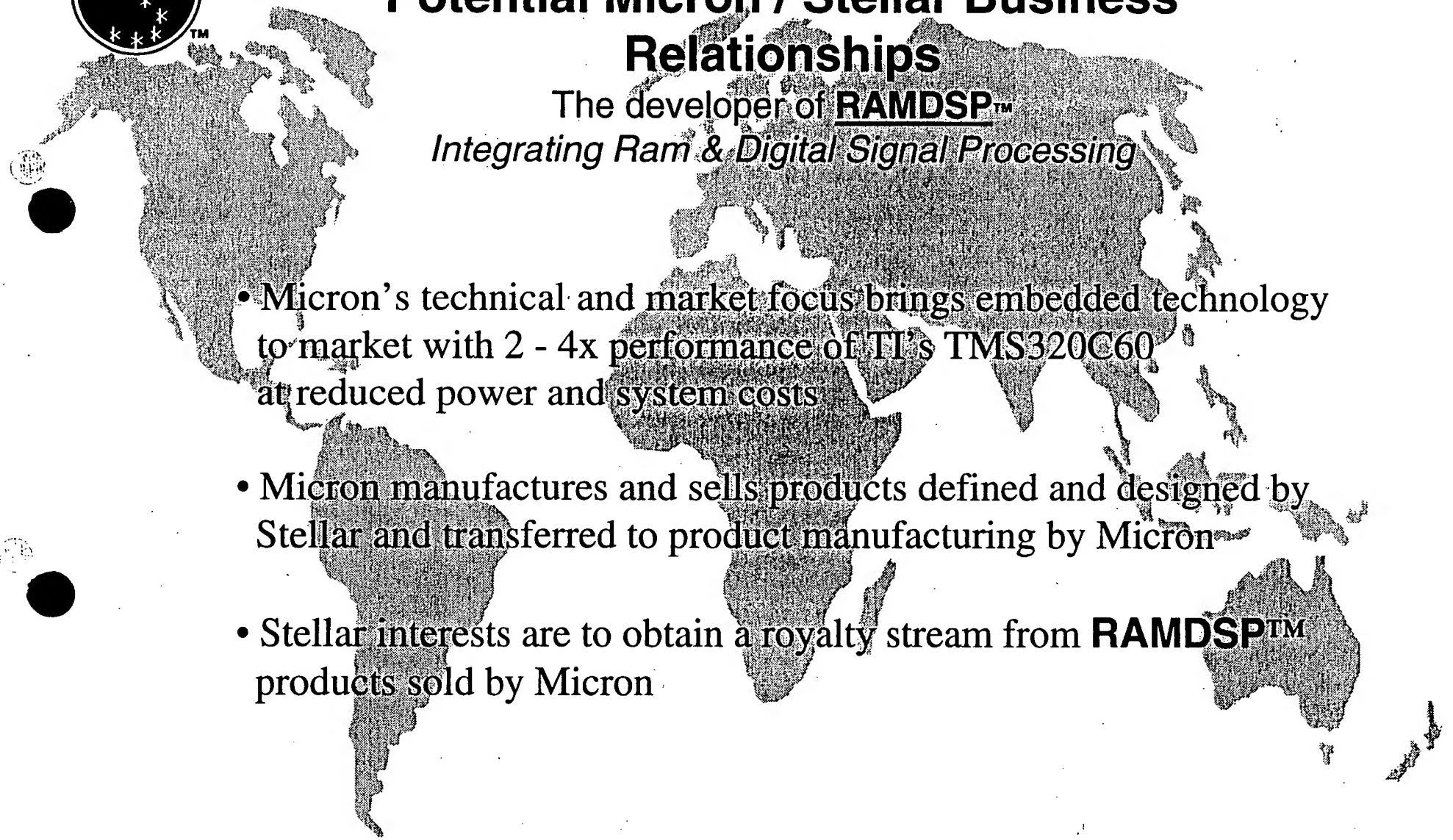
(All of the above require high-performance and substantial amounts of DRAM)

Stellar Business Model

Potential Micron / Stellar Business Relationships

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Micron's technical and market focus brings embedded technology to market with 2 - 4x performance of TI's TMS320C60 at reduced power and system costs
- Micron manufactures and sells products defined and designed by Stellar and transferred to product manufacturing by Micron
- Stellar interests are to obtain a royalty stream from **RAMDSP™** products sold by Micron

Stellar Business Model

Potential Micron / Stellar Business Relationships

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Stellar provides **RAMDSP™** silicon design and software to support high-performance, low-power, low-cost DRAM applications.

- **RAMDSP™** may function as DSP accelerator working in conjunction with a separate front-end controller, or
- **RAMDSP™** implements stand-alone applications that don't require a front-end controller.
- For either of the above, Stellar
  - designs with Micron's tools,
  - sells a license to Micron for **RAMDSP™** technology, and
  - obtains a royalty stream for designs and products sold.
- Stellar will train Micron engineers on **RAMDSP™** software tools and support custom DSP library development.

Stellar Business Model

Milestones and Costs

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

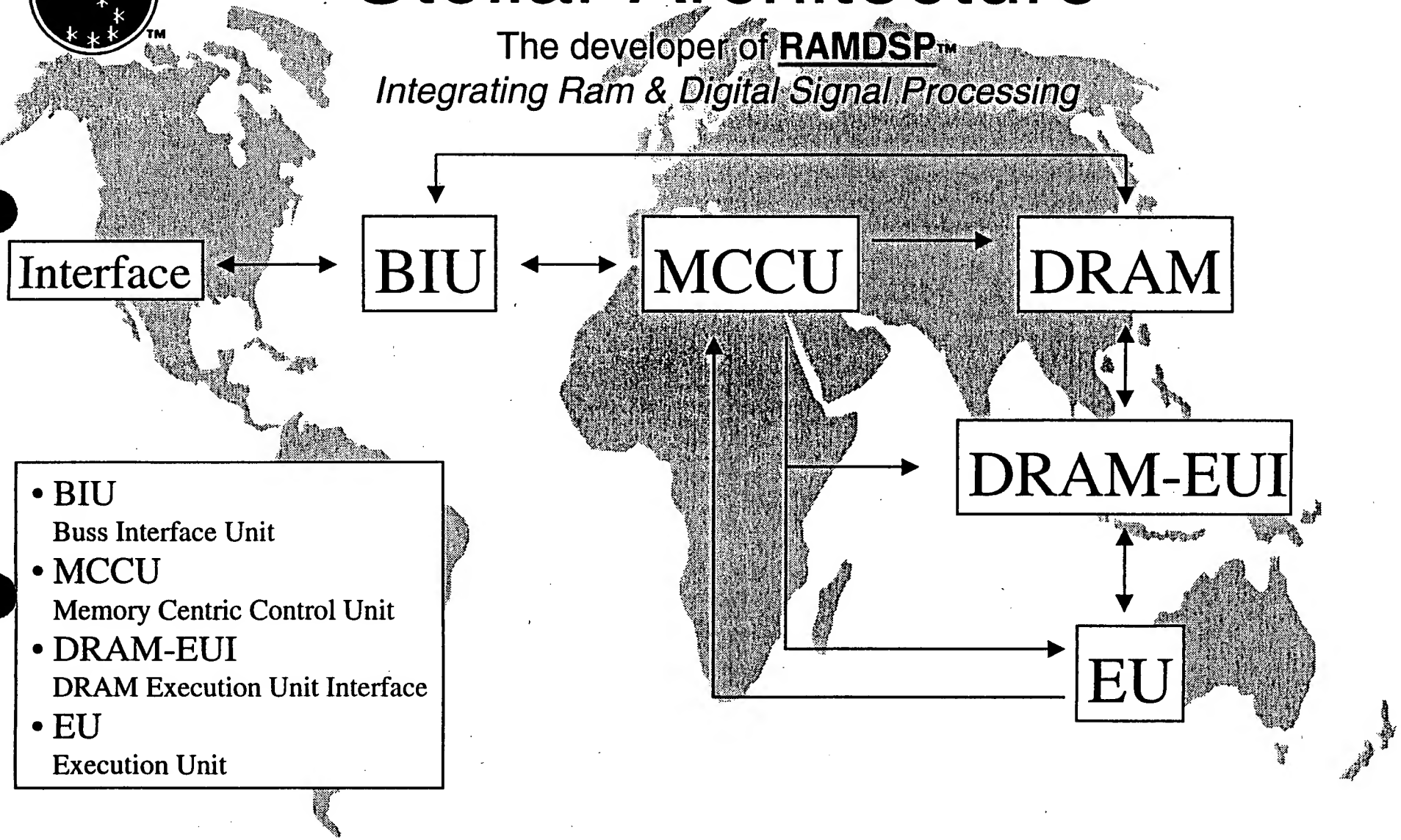
- Q4/97 Functional Specification for MPEG Application
- Q1/98 Functional Simulator and Assembler $650,000.00
  - Architecture Specification for MPEG Application Complete
- Q2/98 Simulator and Behavioral RTL verified, $650,000.00
- Q1,Q2/98 MPEG Application and Market Development $450,000.00
- Q4/98 Software Tools plus MPEG port complete $1.6 million
- Q1/99 Prototype Silicon $3.5 million

(above funds prepay part of IP license and royalties)

Stellar Architecture

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



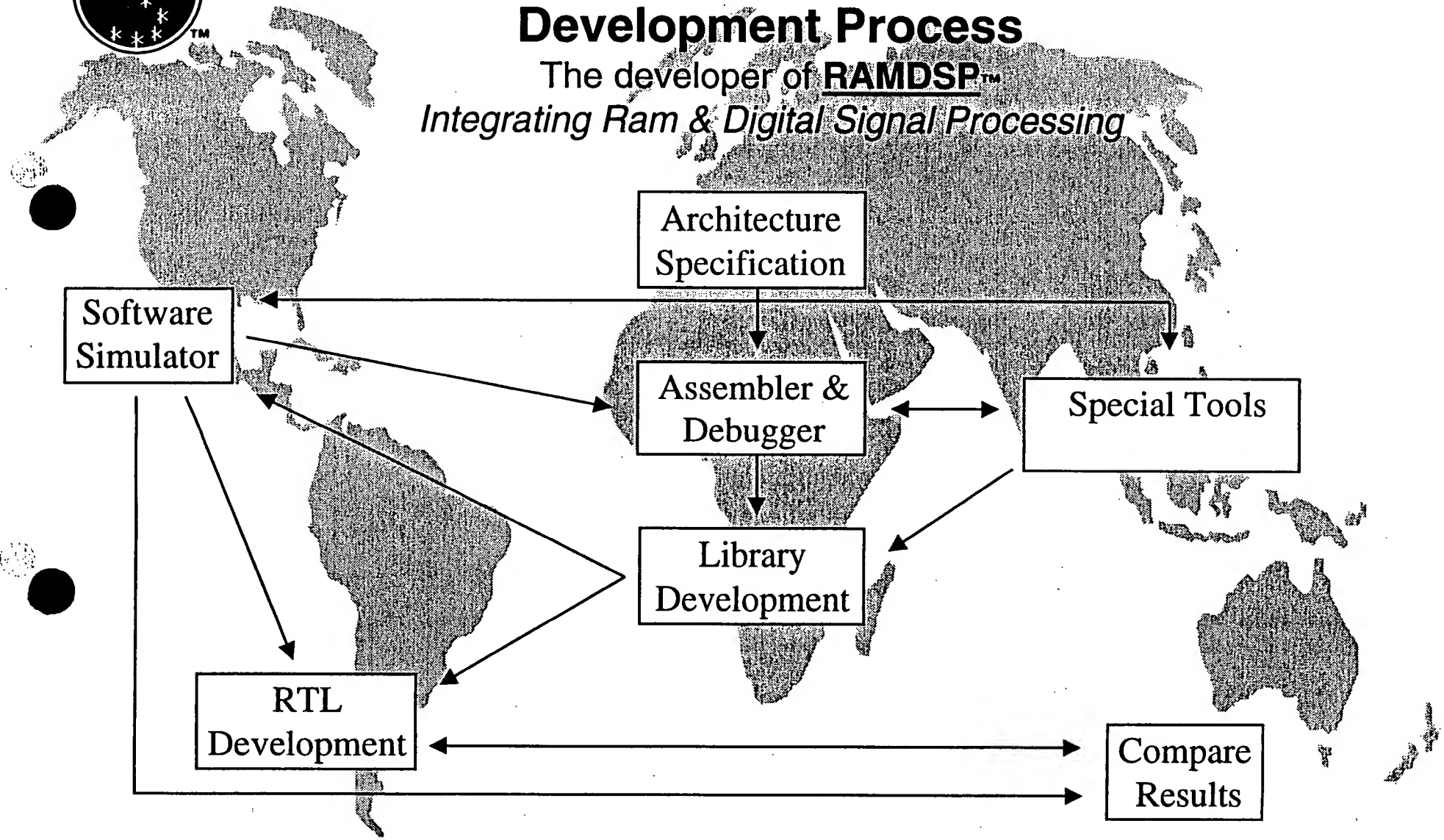
- BIU
  Buss Interface Unit
- MCCU
  Memory Centric Control Unit
- DRAM-EUI
  DRAM Execution Unit Interface
- EU
  Execution Unit

Stellar Architecture

Development Process

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

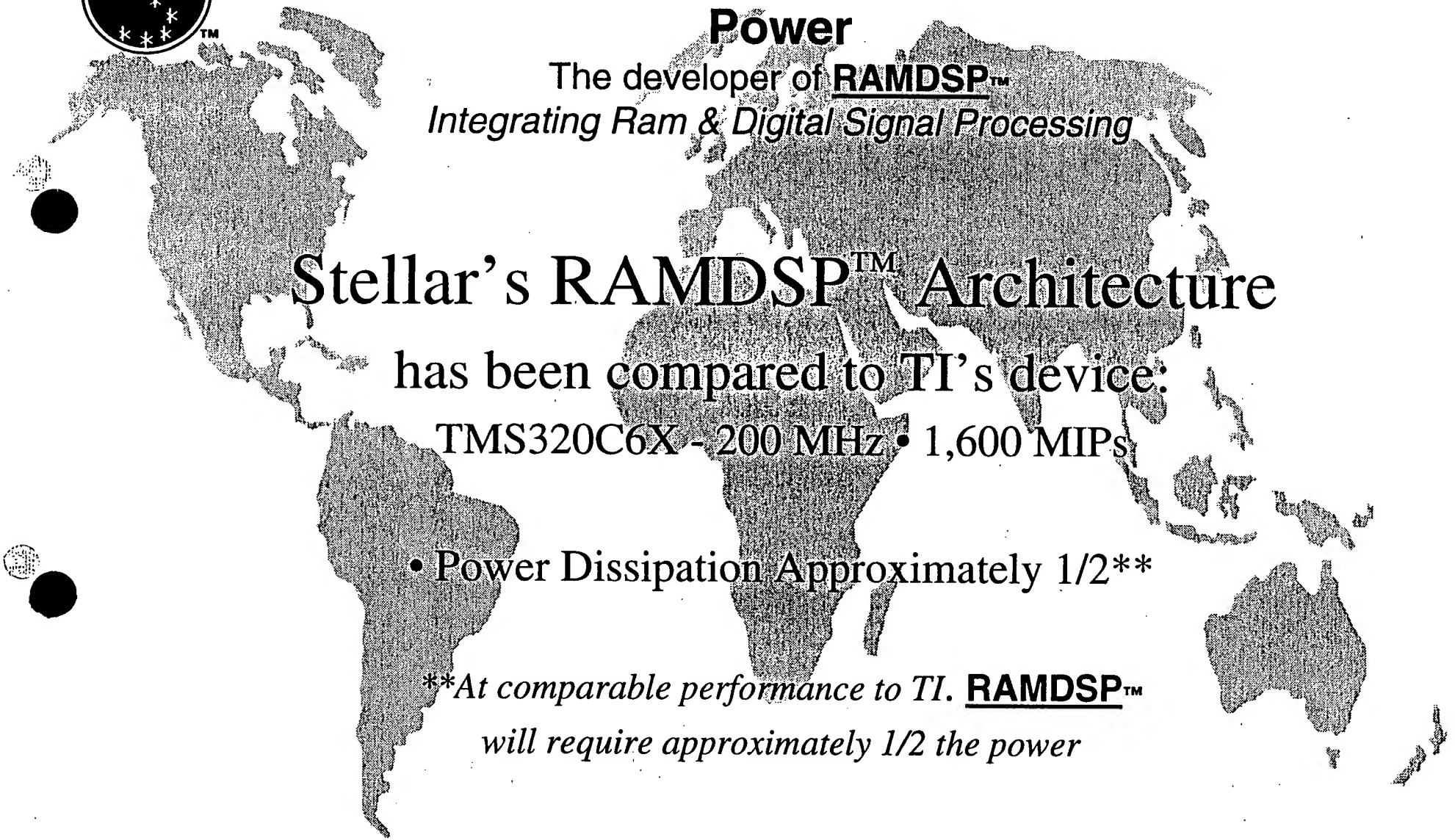


Stellar Cost/Performance

Power

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar's RAMDSP™ Architecture

has been compared to TI's device:

TMS320C6X - 200 MHz • 1,600 MIPs

• Power Dissipation Approximately 1/2**

At comparable performance to TI.* ***RAMDSP™

will require approximately 1/2 the power

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Stellar Cost/Performance

Processing Speed

RAMDSP™

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Stellar's Architecture RAMDSP™

Has been compared to TI's device:

TMS320C6X - 200 MHz • 1,600 MIPs

- Performance Approximately 1- 4x***

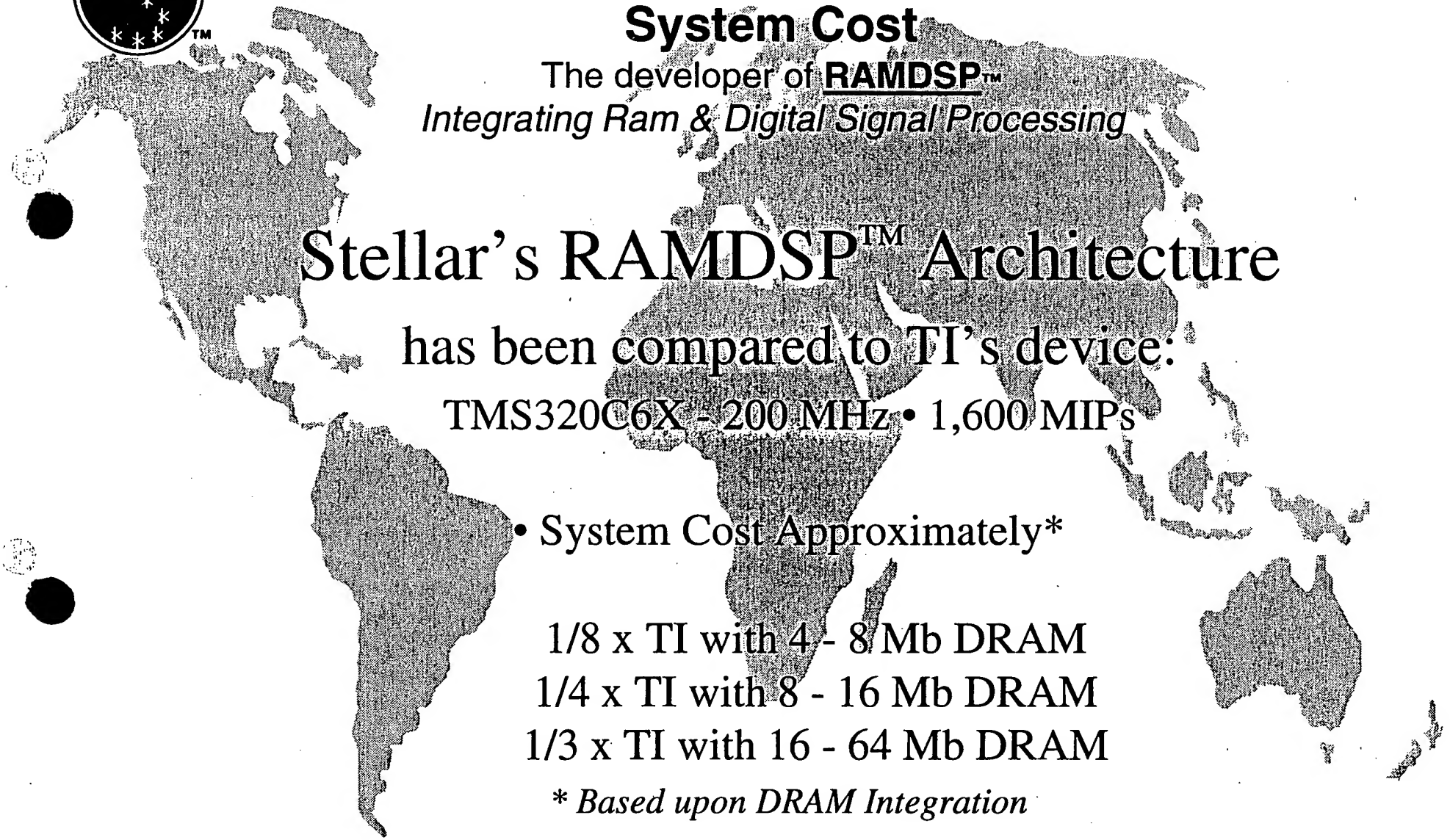
*** **RAMDSP™** *product family will support performance range of 1 to 4 times the performance of TMS320C6X on a single chip*

Stellar Cost/Performance

System Cost

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar's RAMDSP™ Architecture

has been compared to TI's device:

TMS320C6X - 200 MHz • 1,600 MIPs

• System Cost Approximately*

1/8 x TI with 4 - 8 Mb DRAM
1/4 x TI with 8 - 16 Mb DRAM
1/3 x TI with 16 - 64 Mb DRAM

** Based upon DRAM Integration*

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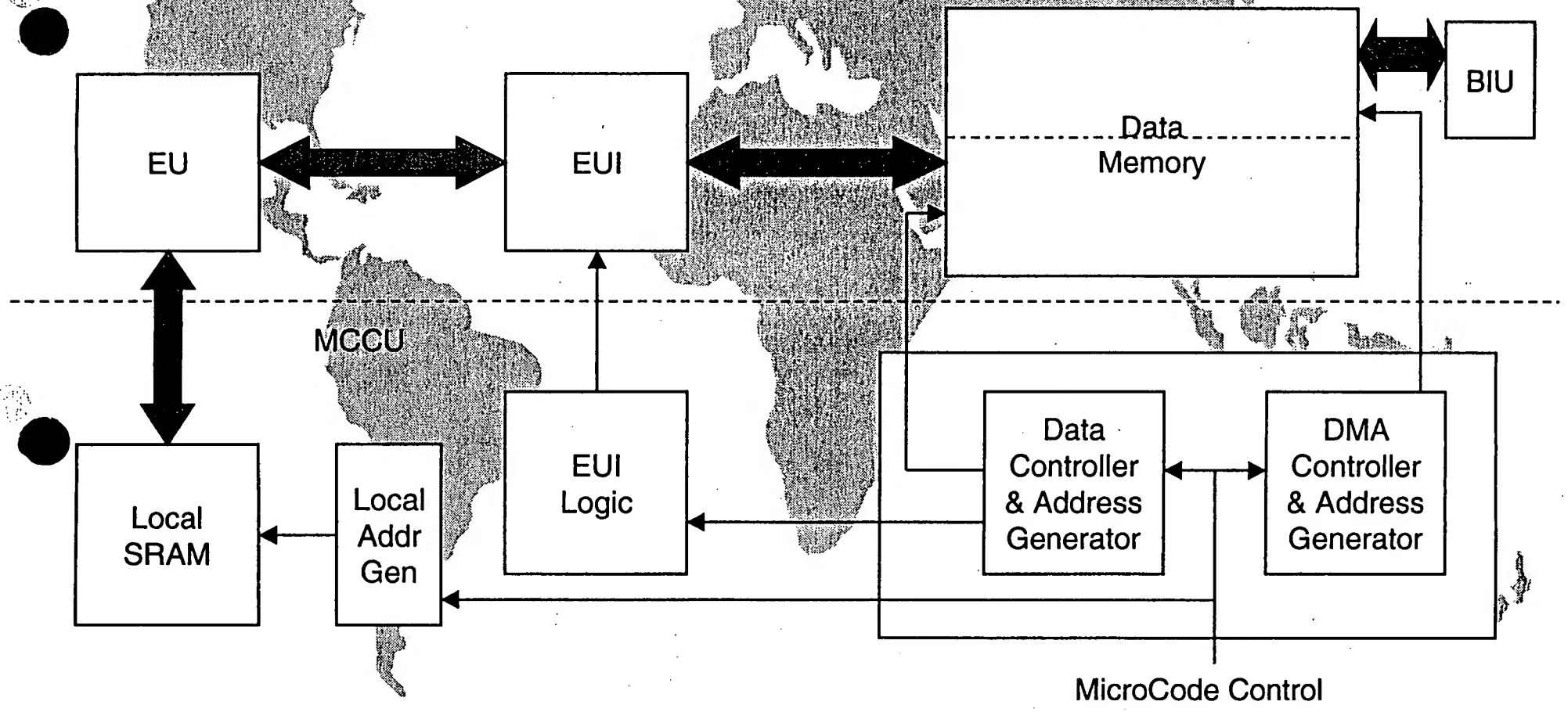
Stellar Architecture

Data Ram & Local Ram

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

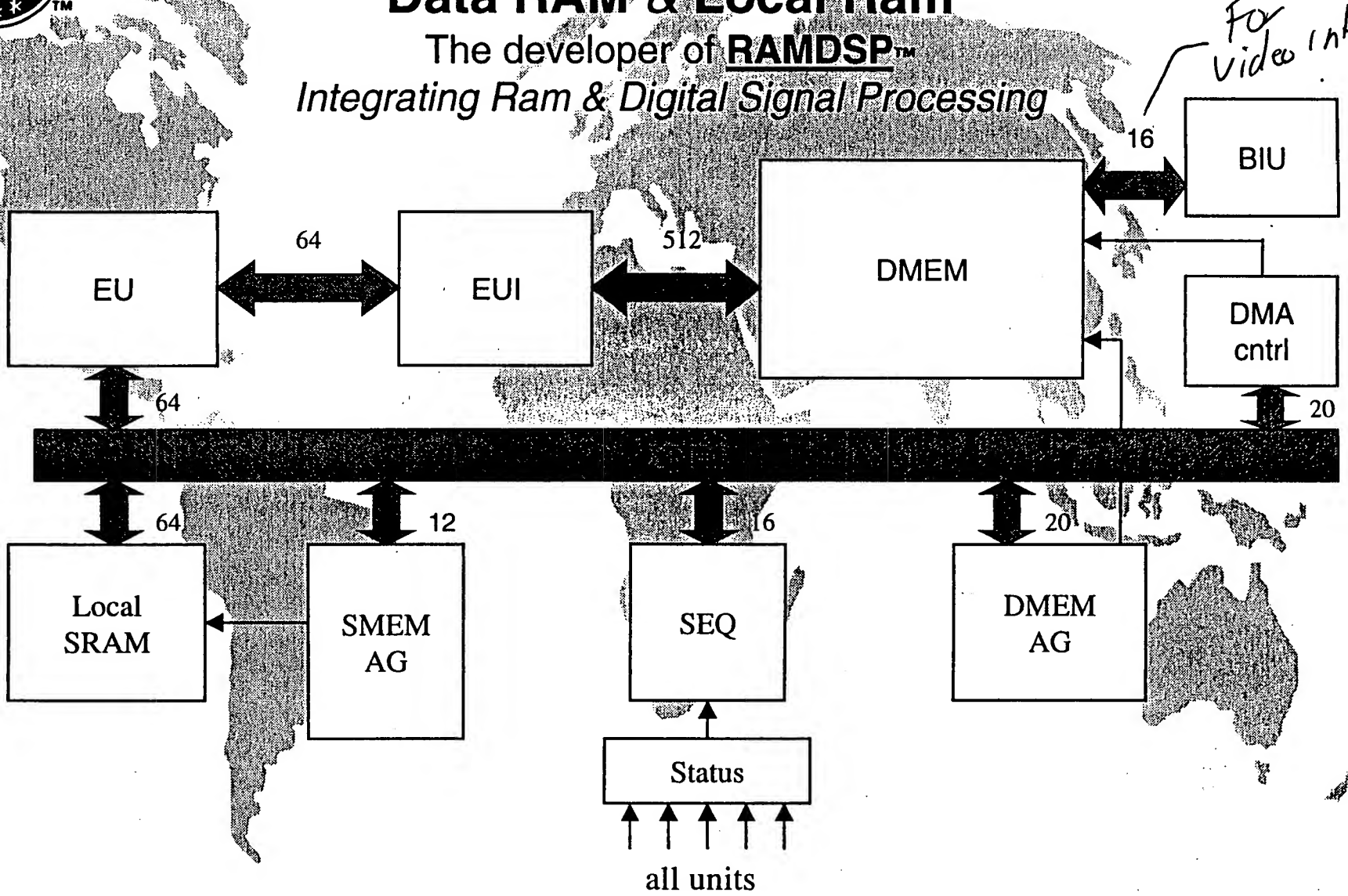


Stellar Architecture

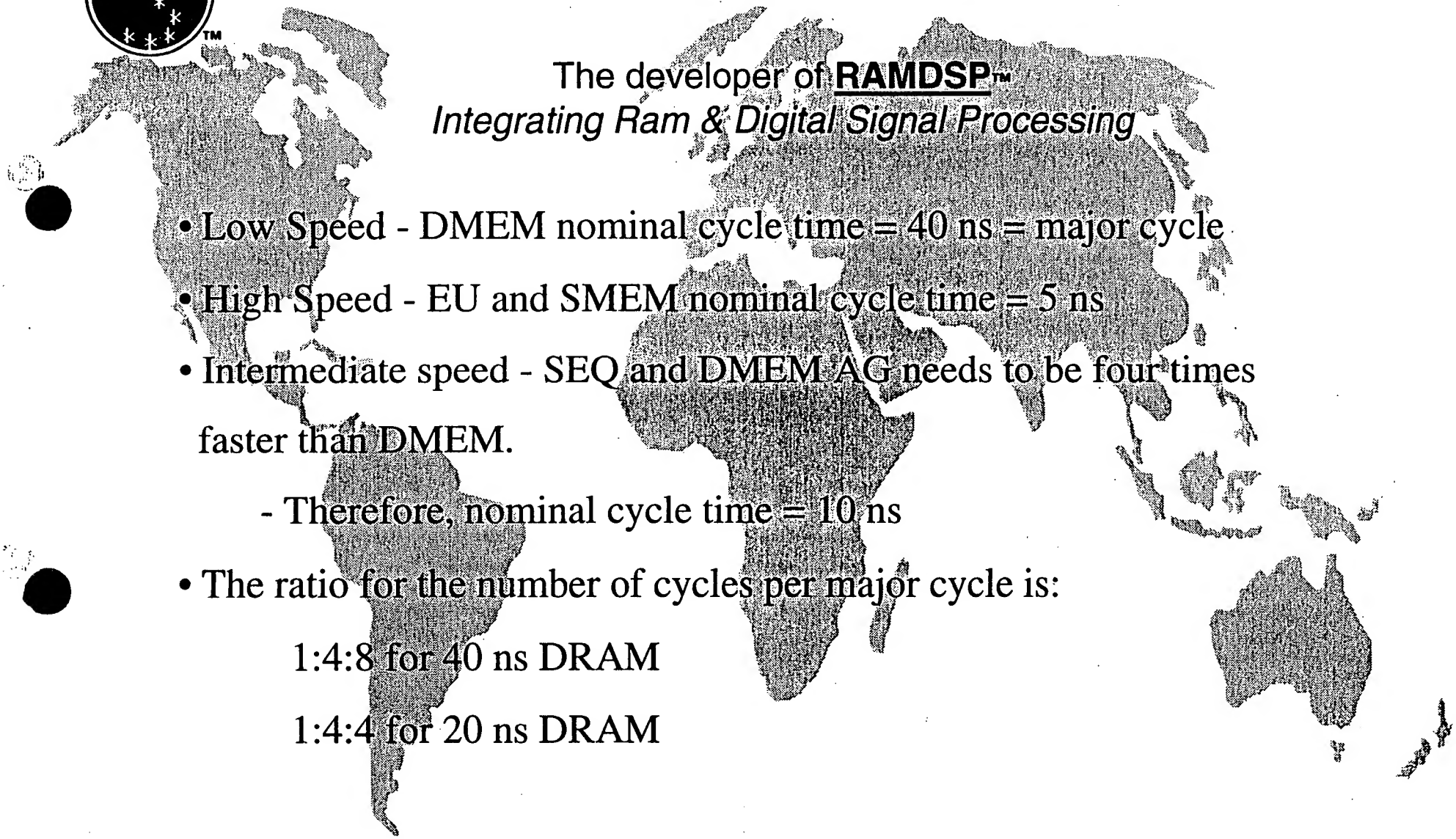
Data RAM & Local Ram

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture



The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing

- Low Speed - DMEM nominal cycle time = 40 ns = major cycle
- High Speed - EU and SMEM nominal cycle time = 5 ns
- Intermediate speed - SEQ and DMEM AG needs to be four times faster than DMEM.
  - Therefore, nominal cycle time = 10 ns
- The ratio for the number of cycles per major cycle is:
  - 1:4:8 for 40 ns DRAM
  - 1:4:4 for 20 ns DRAM

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Stellar Architecture

Memory Centric Controller Unit cont.

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

RAMDSP technology applies to both DRAM and SRAM data memory

- Memory Addressing for Execution Unit
- Operation Control Fields
- Execution Unit timing
- Memory interface unit timing and control
- Control for reconfiguring and sharing memory

Stellar Architecture

Memory Centric Controller Unit cont.

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Power Management Control
- Addressing for Multiple Memory Blocks, Multiple Execution Units, and Memory I/O
- Provision for Fast Local Storage
- Full Support for Conditional Execution
- Provides Complete Built-in Self Test Capabilities
  - reduces manufacturing costs
  - implements control information for repair

Stellar Architecture

MCCU Interface Controls

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

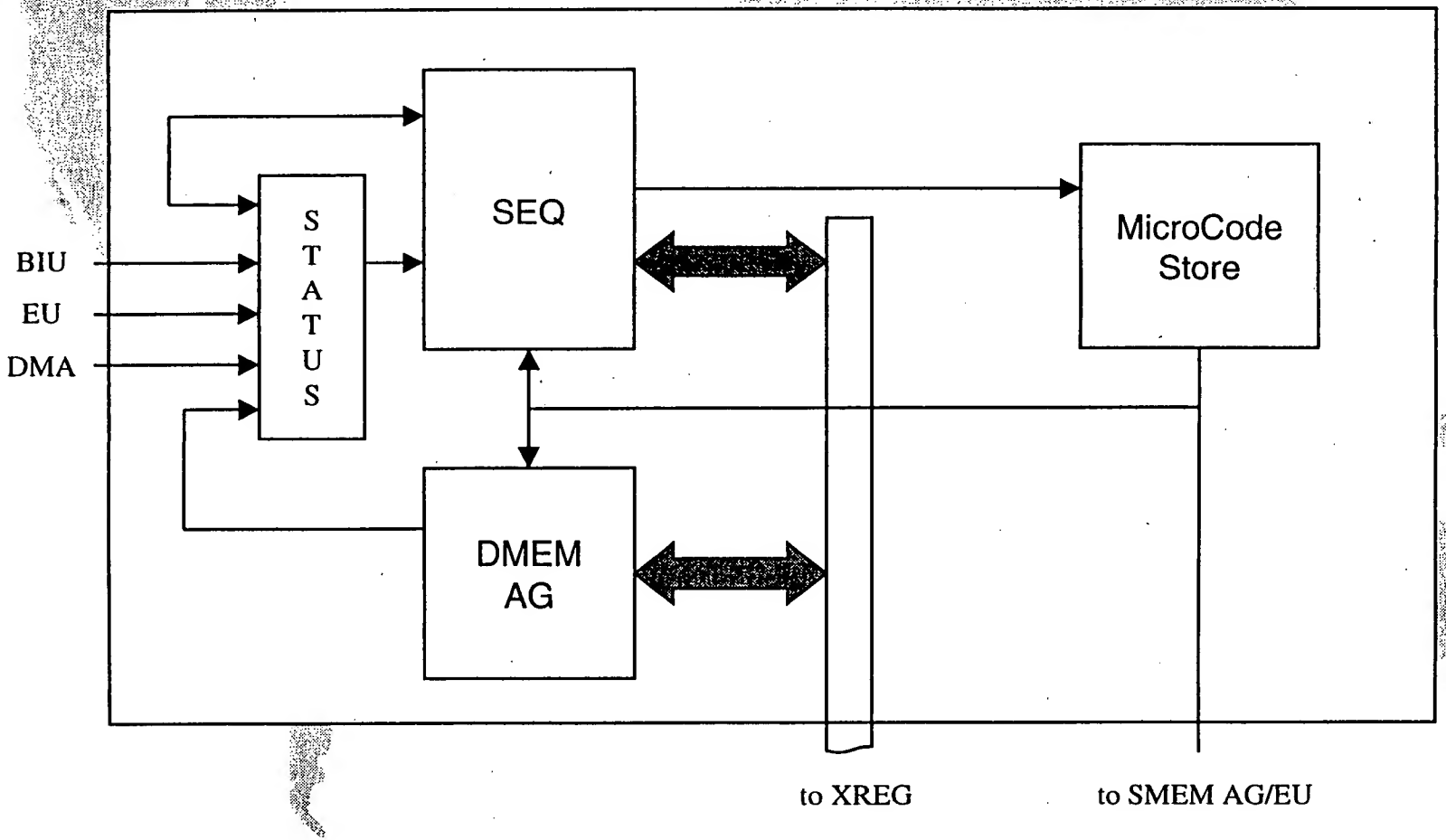
- Status Block Information Control from Engine to Core processor
- Interrupt Handling Processor ⟷ Engine
- Engine To Engine Communications
  - Multi-processor support
  - Stand-alone processing
  - Status
  - Interrupts
- Support for Memory Mapped Instructions from Core processor to Engine

Stellar Architecture

MCCU Block Diagram

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

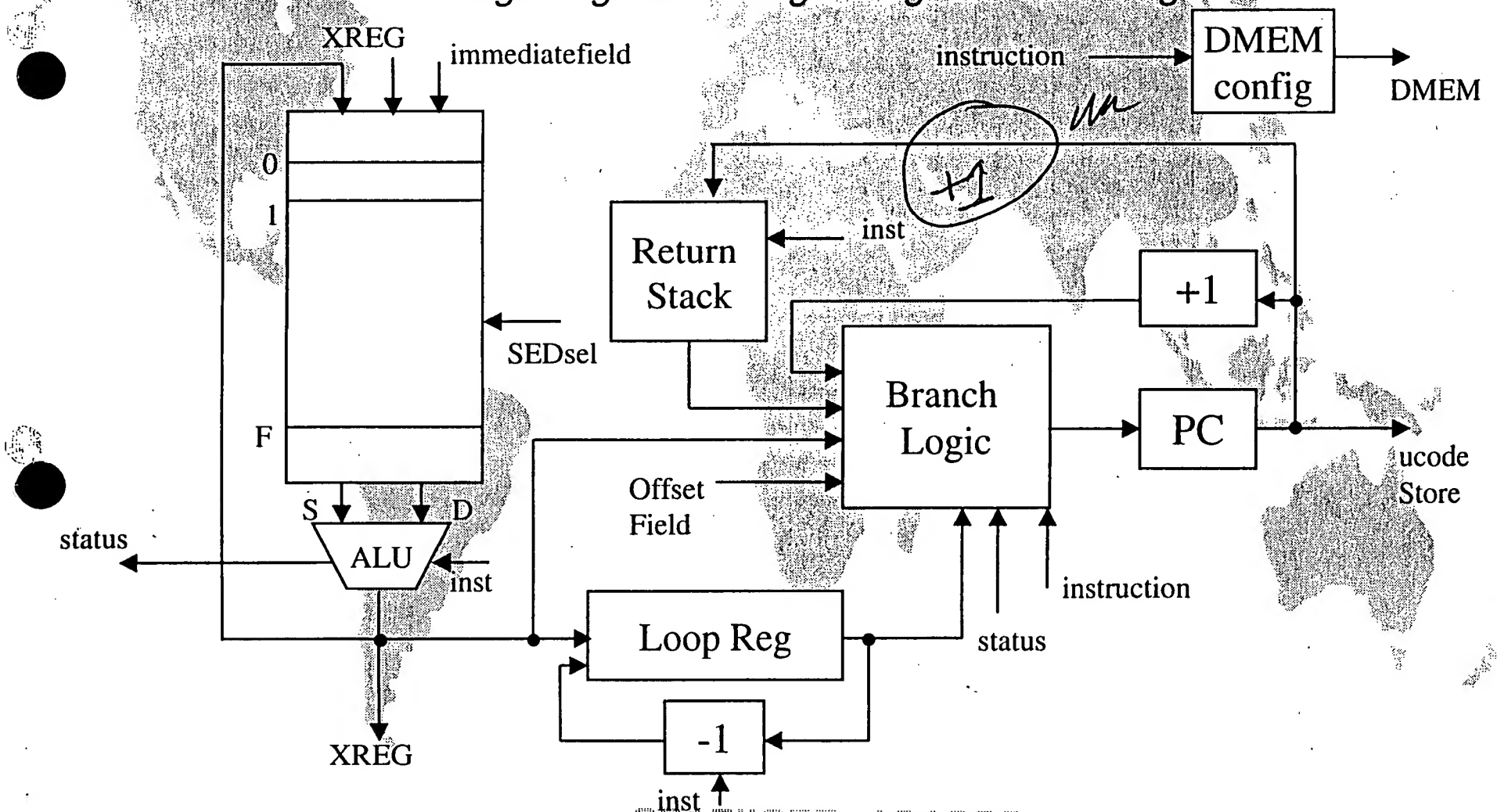


Stellar Architecture

MCCU Sequence Controller

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

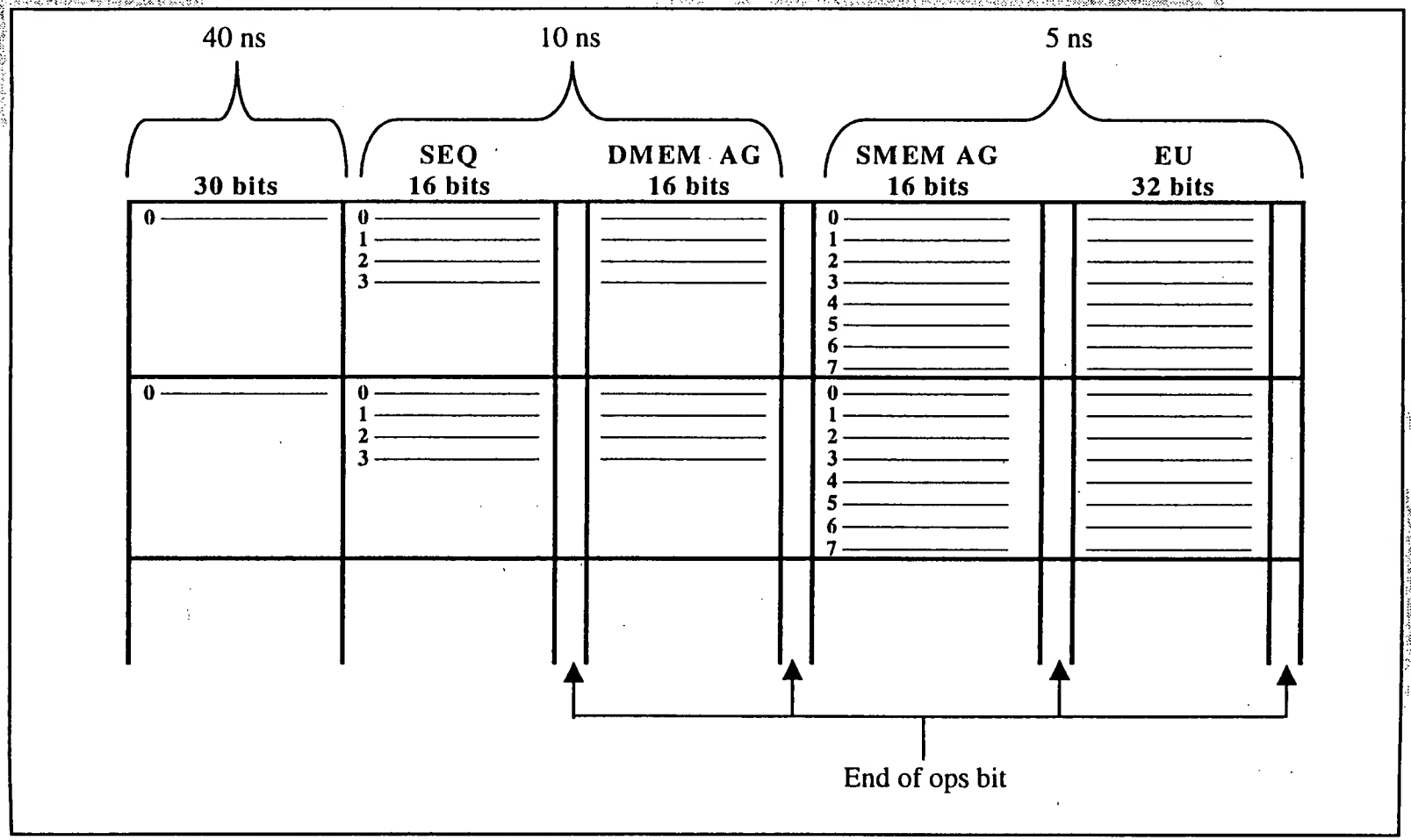


Stellar Architecture

MicroCode Store Segmentation

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

MicroCode Store

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

End of Operations Bit

- The EOO Bit is set by the assembler
- When the EOO Bit is encountered, that MicroCode block is idle until the start of the next major cycle
- Note that the units are idle during a NOP

Example of EOO Bit for DMEM AG

Assembler Code	Machine Code	EOO Bit
inc 3, setaddr	1 2 3 0	1
nop	0 0 0 0	0
nop	0 0 0 0	0
nop	0 0 0 0	0

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Stellar Architecture

Data Ram Partitioning

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

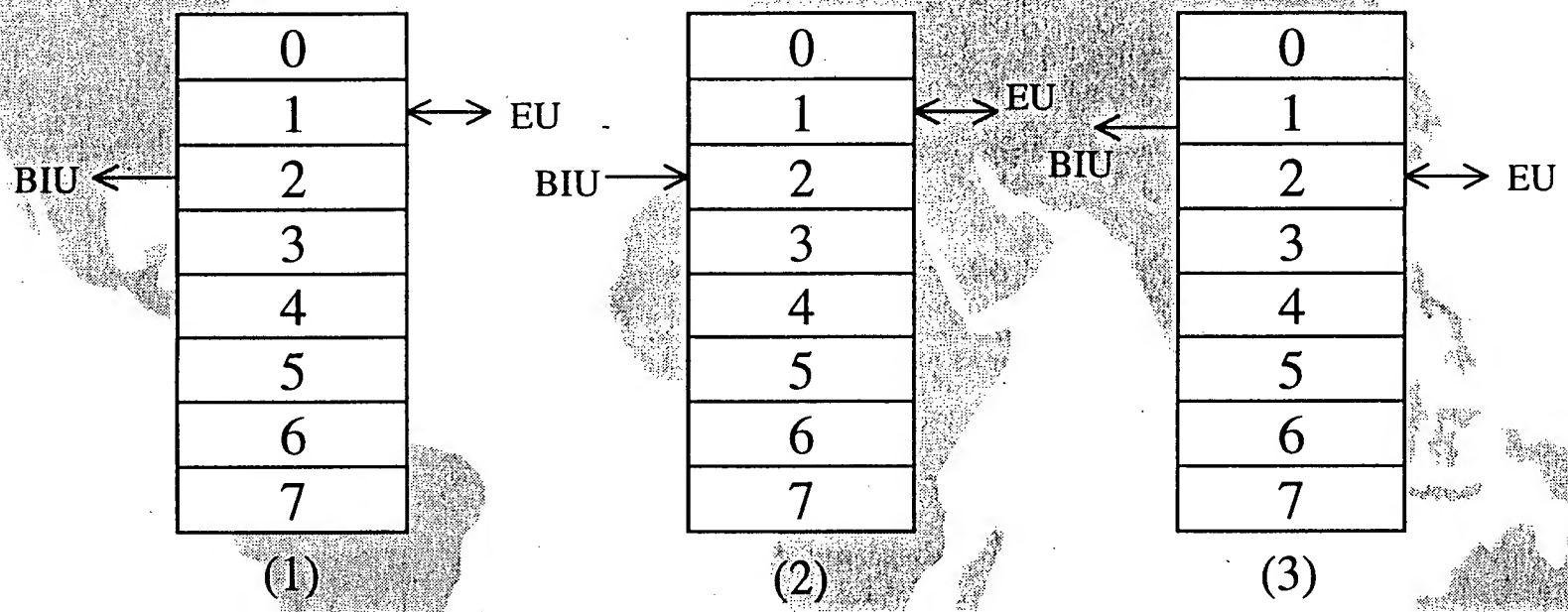
- Data Ram addressed in 8 assignable segments
- Execution Unit and Bus Interface Unit swap data segments transparently
- Fixed segments preserve algorithm state
- MCCU controls reconfiguration and coordinates processing with I/O

Stellar Architecture

Data Ram Partitioning

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



1. Current execution with segment 1 while last results are unloaded from segment 2.

2. Execution continues with segment 1 while next data is loaded into segment 2.

3. Segments are reassigned - execute with segment 2 while previous results are unloaded from segment 1.

Stellar Architecture

Bus Interface Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Provides a high bandwidth programmable interface to standard and custom busses
- Shares control with the MCCU
- Direct path to DRAM I/O Blocks

Stellar Architecture

Bus Interface Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Maintains high bandwidth communication between BIU and DRAM block
- Support for various standards
  - Synchronous DRAM
  - EDO
  - Rambus
  - PCI
- Simple interface can substitute for BIU, e.g., standard memory buss interface

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Stellar Architecture

Execution Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

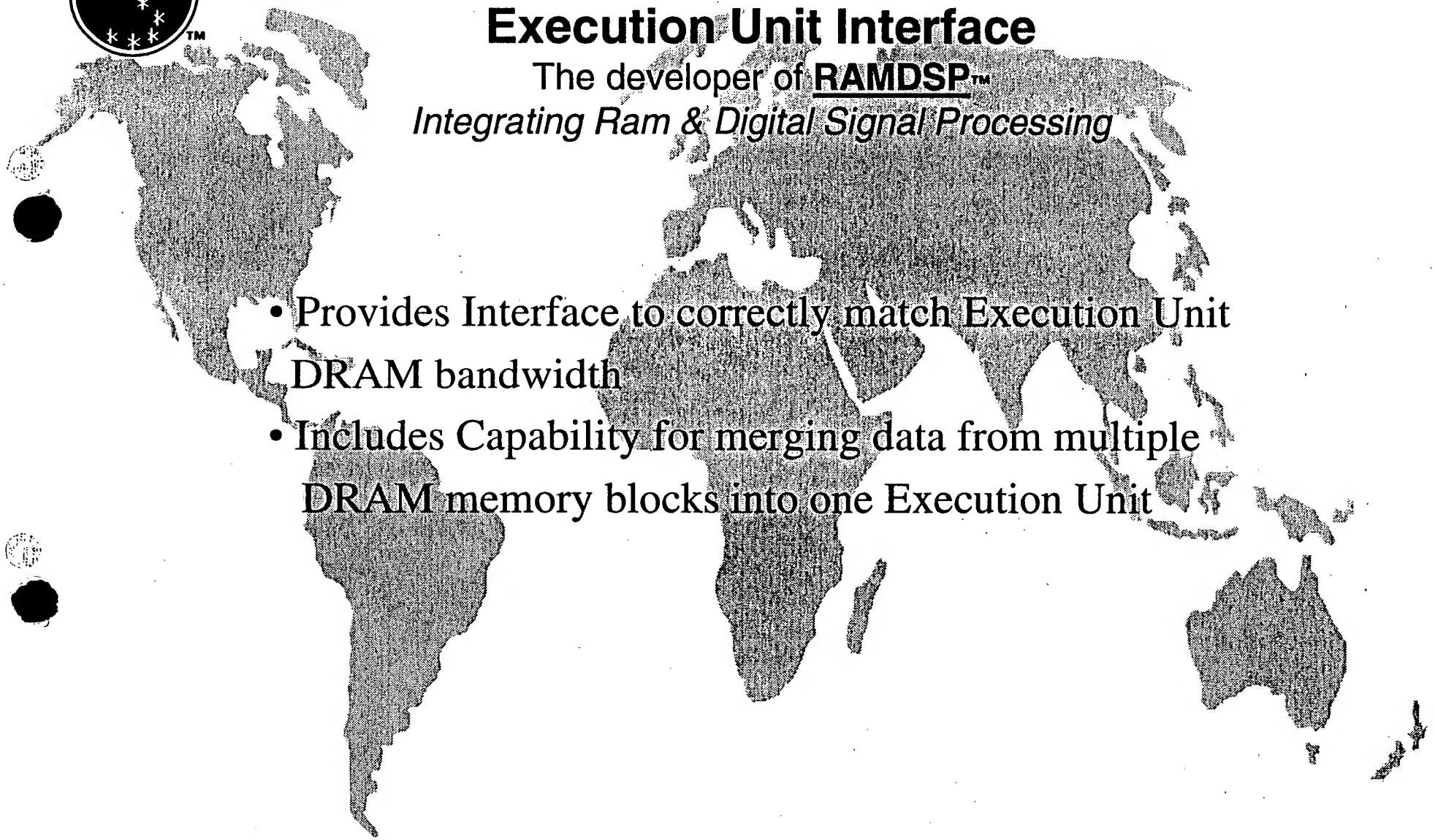
- Extendable Architecture
- Two ⟷ Eight Way SIMD
- Local Memory Support for Execution Units
- Branch and Interrupt Status Feedback To MCCU

Stellar Architecture

Execution Unit Interface

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



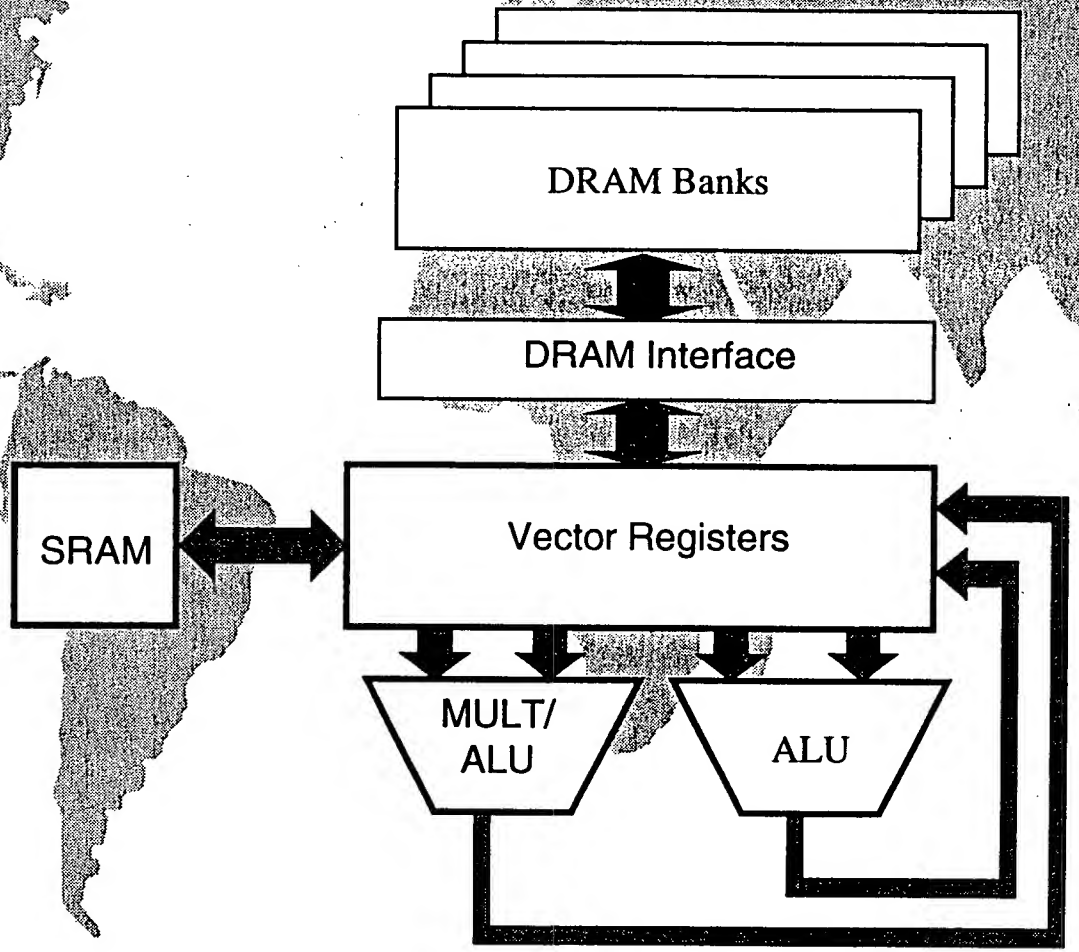
- Provides Interface to correctly match Execution Unit DRAM bandwidth
- Includes Capability for merging data from multiple DRAM memory blocks into one Execution Unit

Stellar Architecture

Parallel SIMD Style Execution Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

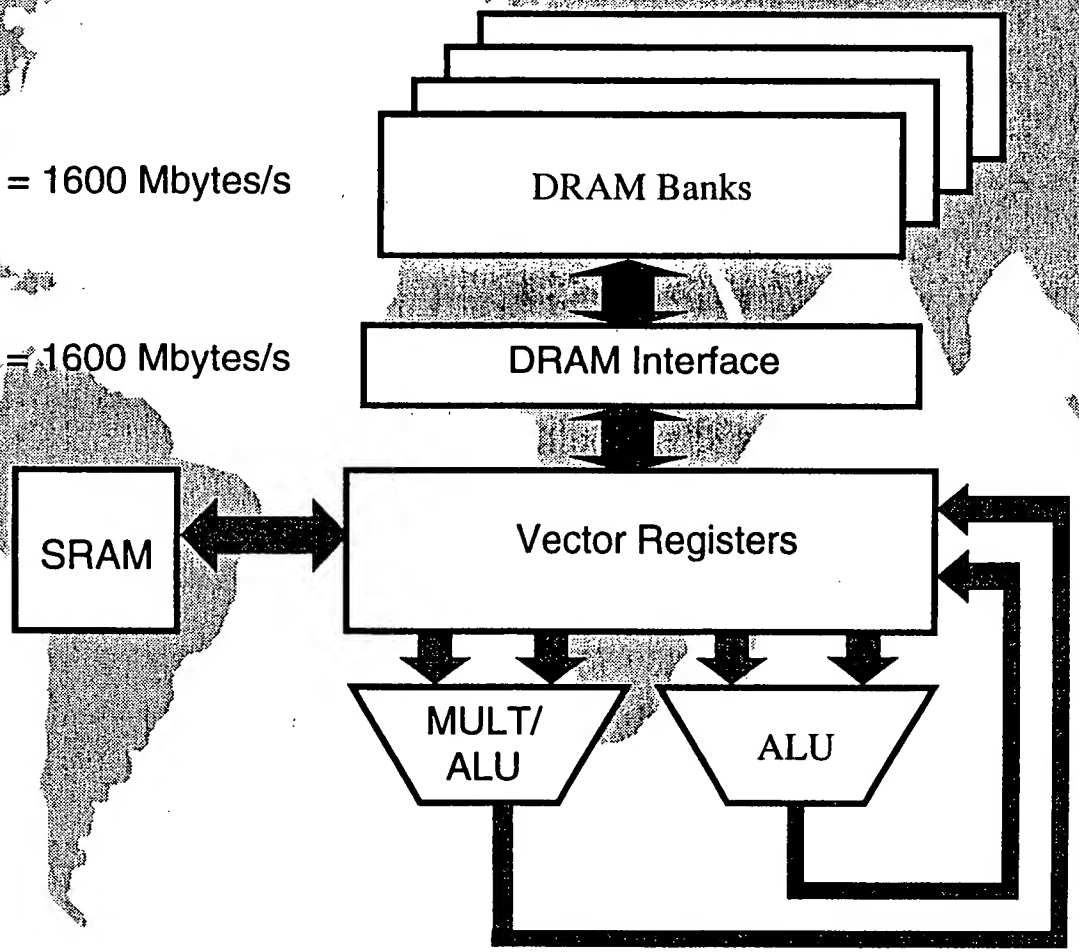
Matched Data Rates

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

25 MHz x 512-bits = 1600 Mbytes/s

200 MHz x 64-bits = 1600 Mbytes/s



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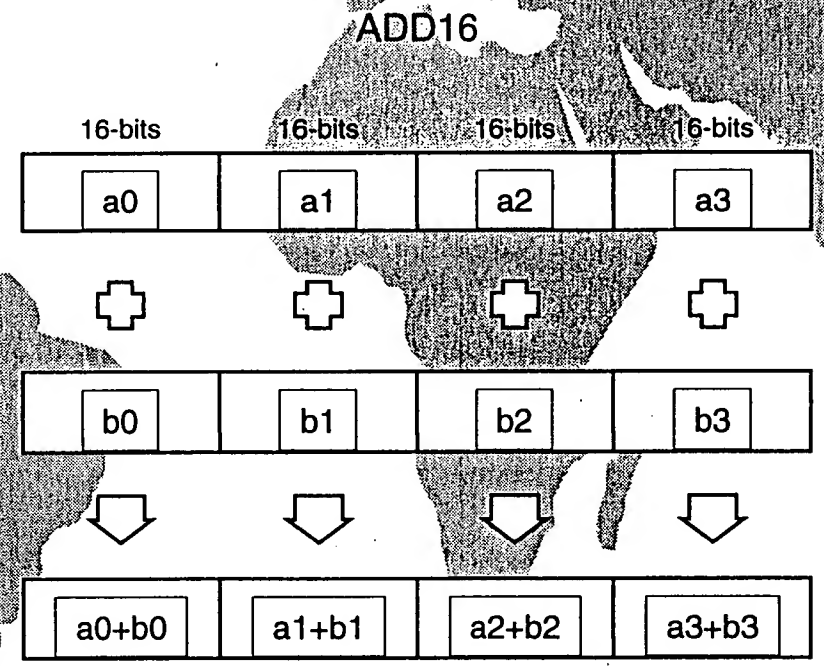
Stellar Architecture

Parallel SIMD Execution Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

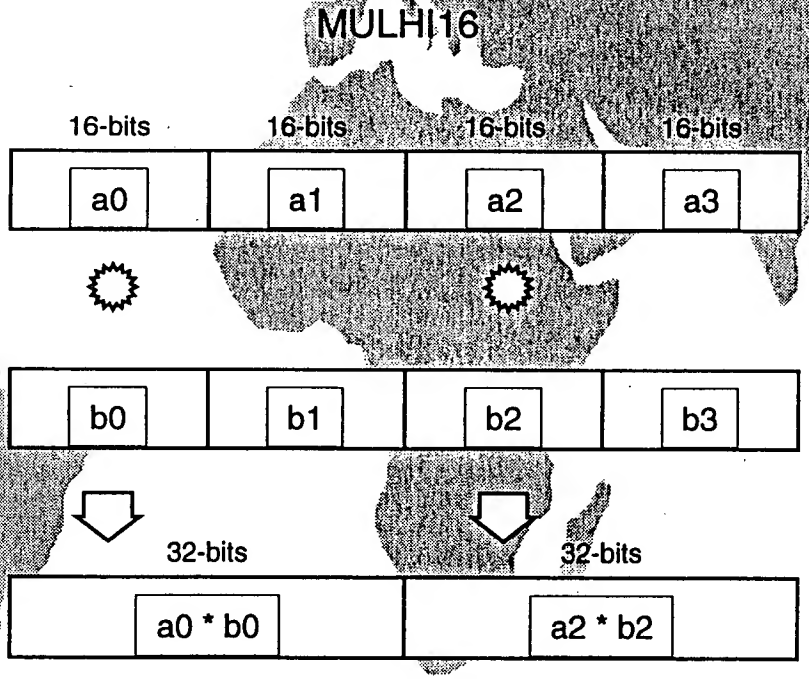


Stellar Architecture

Parallel SIMD Execution Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

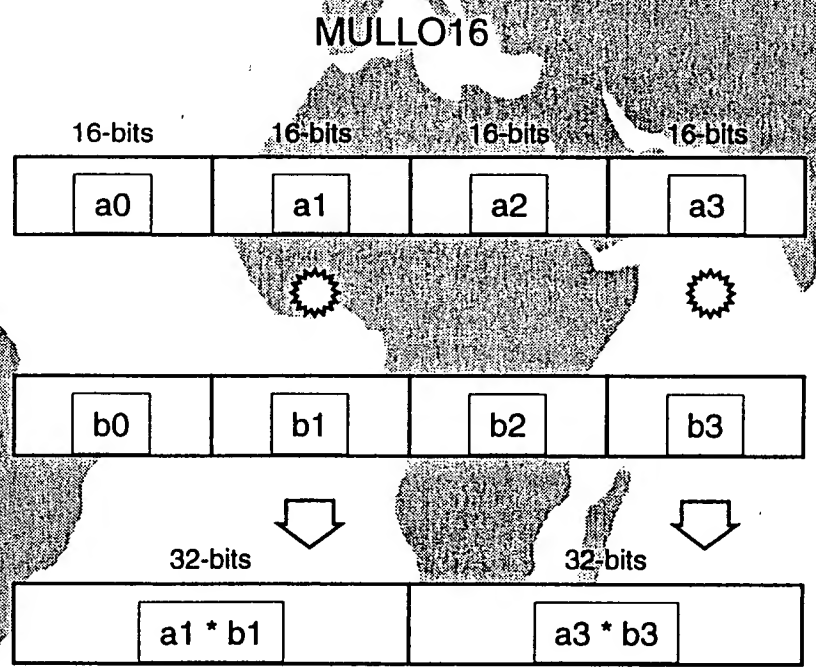


Stellar Architecture

Parallel SIMD Execution Unit

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

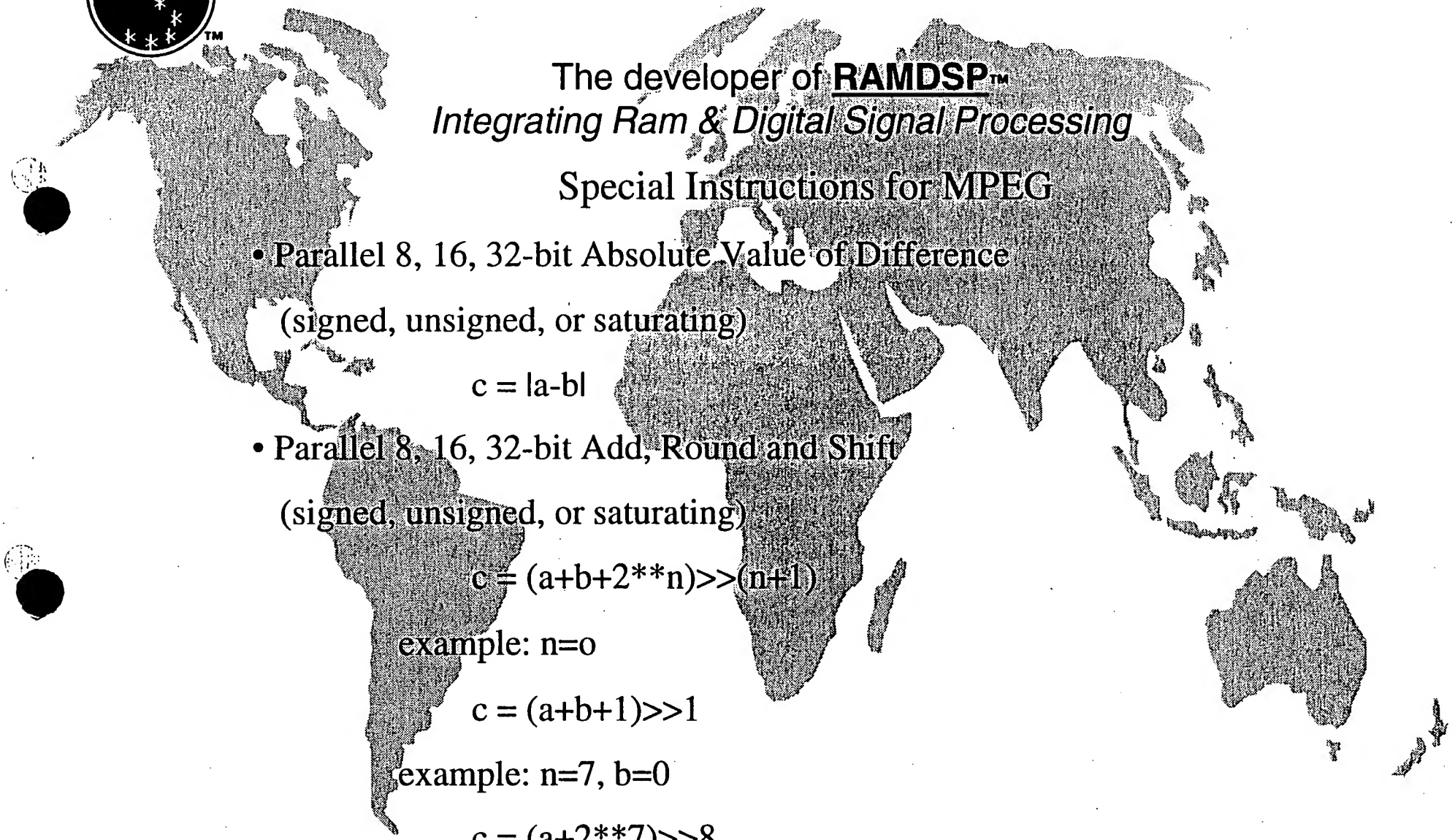
SIMD uCode Instructions

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Multiplier can do some Adder operations
- Parallel 8, 16, 32-bit ADD, COMP, SHIFT (signed, unsigned, or saturating)
- Parallel 8, 16-bit MUL (to double width) (odd or even; signed or unsigned)
- 64-bit AND, OR, XOR
- Parallel PACK and UNPACK (odd or even fields)
- MOVE and MERGE (under mask)
- LDZero, LDOne (for normalization and compression)

Stellar Architecture



The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Special Instructions for MPEG

- Parallel 8, 16, 32-bit Absolute Value of Difference

  (signed, unsigned, or saturating)

  c = |a-b|

- Parallel 8, 16, 32-bit Add, Round and Shift

  (signed, unsigned, or saturating)

  c = (a+b+2**n)>>(n+1)

  example: n=o

  c = (a+b+1)>>1

  example: n=7, b=0

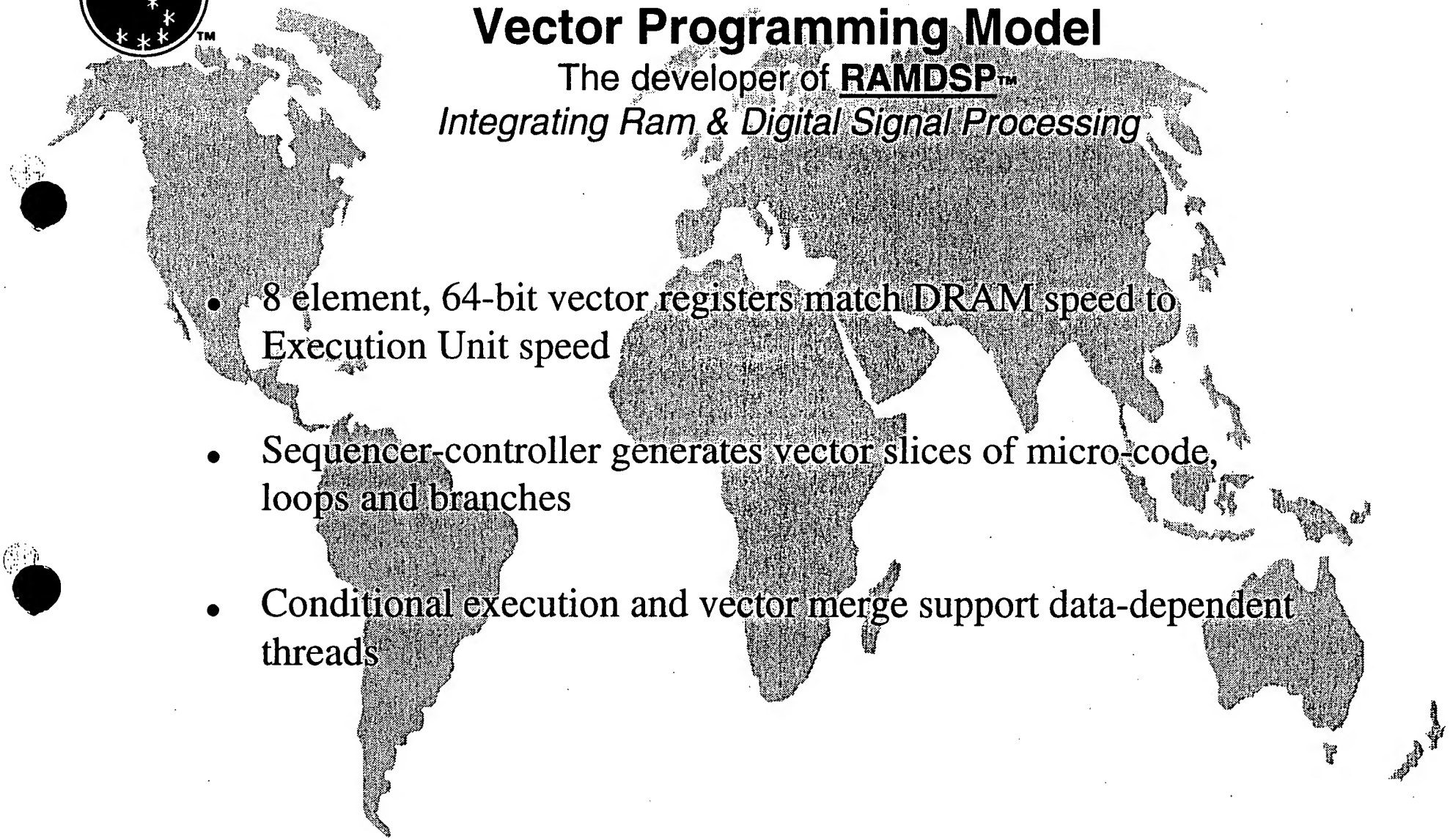
  c = (a+2**7)>>8

Stellar Architecture

Vector Programming Model

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



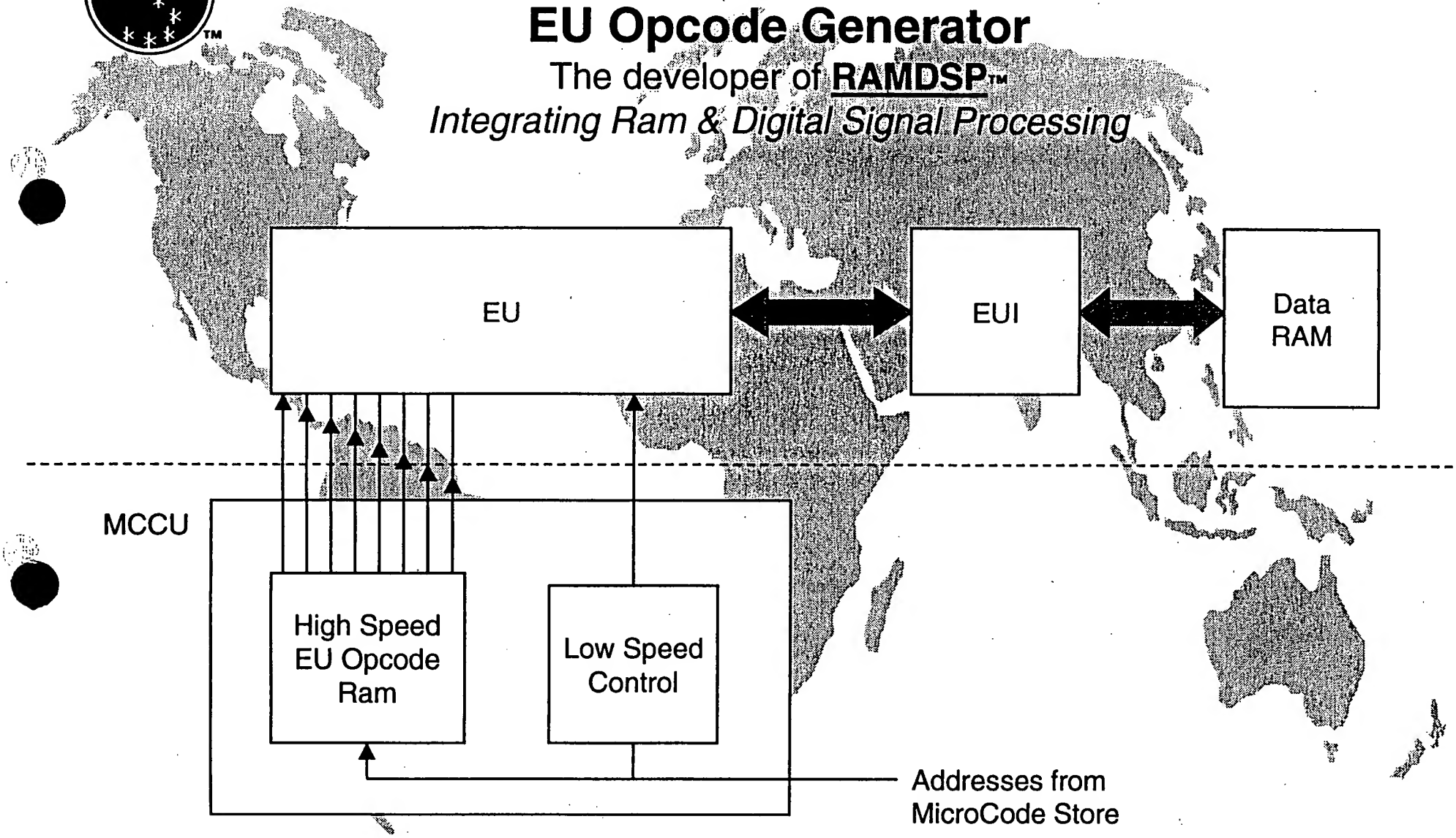
- 8 element, 64-bit vector registers match DRAM speed to Execution Unit speed
- Sequencer-controller generates vector slices of micro-code, loops and branches
- Conditional execution and vector merge support data-dependent threads

Stellar Architecture

EU Opcode Generator

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



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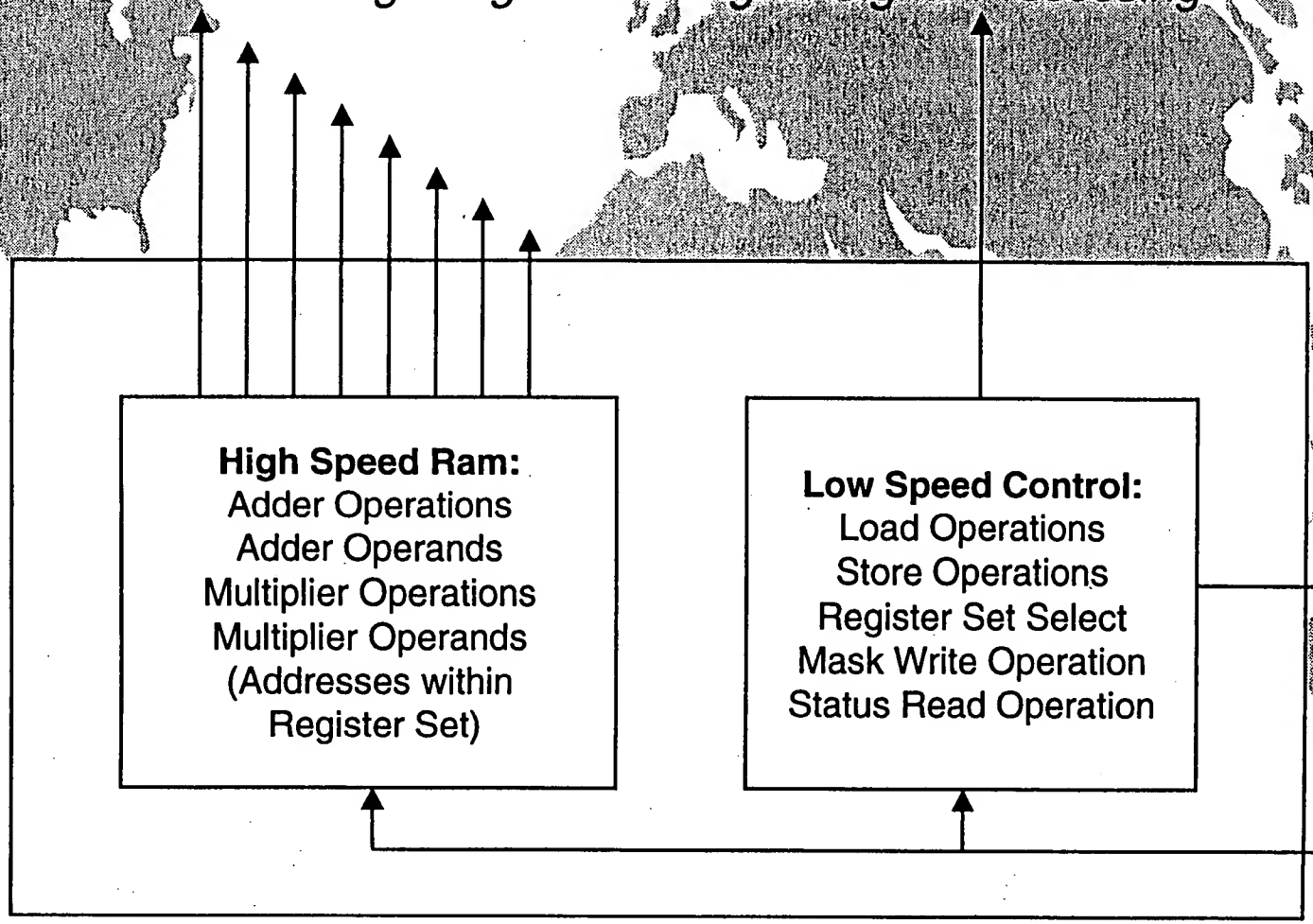
Stellar Architecture

EU Opcode Generator

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

Peak Execution Rates

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- 200 MHz Execution Unit / 25 MHz DRAM (nominal)

- 4 x (8-bit Mult + 16-bit Add) = 8 x 200 MHz = 1600 Mops or
- 2 x (16-bit Mult + 32-bit Add) = 4 x 200 MHz = 800 Mops or
- 8 x (16-bit Add) = 8 x 200 MHz = 1600 Mops or
- 16 x (8-bit Add) = 16 x 200 MHz = 3200 Mops

- Memory Bandwidth
  8 Bytes x 200 MHz = 1600 M Byte/s

  (per 64-bit data path)

- Depending on DRAM technology, up to 4 64-bit data paths and execution units may be accommodated

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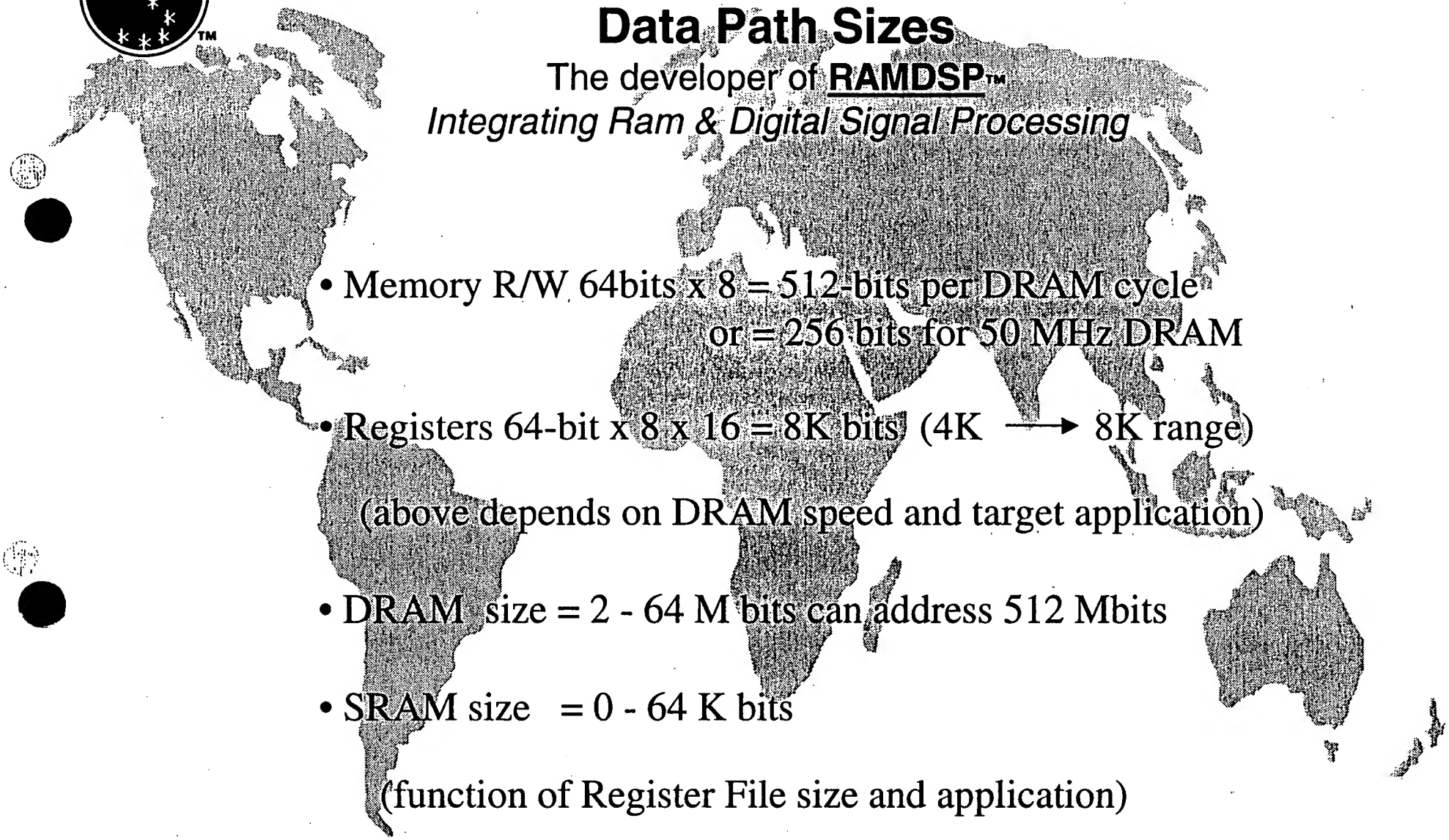
Stellar Architecture

Data Path Sizes

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Memory R/W 64bits x 8 = 512-bits per DRAM cycle
  or = 256 bits for 50 MHz DRAM
- Registers 64-bit x 8 x 16 = 8K bits (4K → 8K range)

(above depends on DRAM speed and target application)

- DRAM size = 2 - 64 M bits can address 512 Mbits
- SRAM size = 0 - 64 K bits

(function of Register File size and application)

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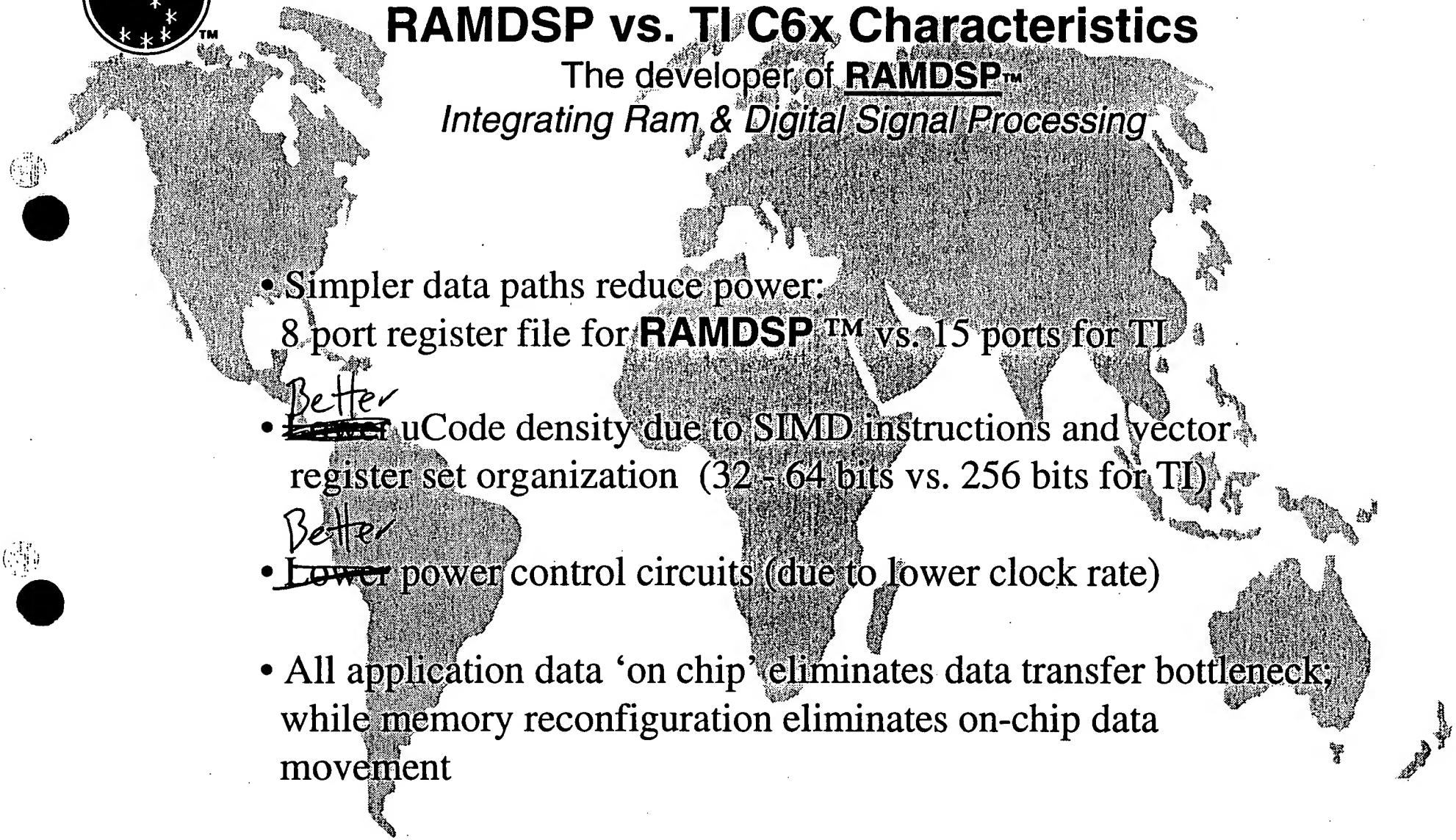
Stellar Architecture

RAMDSP vs. TI C6x Characteristics

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Simpler data paths reduce power:
  8 port register file for **RAMDSP ™** vs. 15 ports for TI
- Better ~~Lower~~ uCode density due to SIMD instructions and vector register set organization (32 - 64 bits vs. 256 bits for TI)
- Better ~~Lower~~ power control circuits (due to lower clock rate)
- All application data 'on chip' eliminates data transfer bottleneck; while memory reconfiguration eliminates on-chip data movement

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Stellar Architecture

RAMDSP vs. TI C6x Characteristics

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Flexible SIMD style execution allows additional data parallelism and 2 - 4x execution speed

- TI: 2 x 32-bit adds per clock
  and
  2 x 16-bit mults

- RAMDSP ™ : 2 x 32-bit adds per clock
  4 x 16-bit adds or
  8 x 8-bit adds
  and
  2 x 16-bit mults
  4 x 8-bit mults

  or

  4 x 32 - bit adds
  8 x 32 - bit adds
  16 x 8 - bit adds

- And **RAMDSP** ™ can support 2 - 4x the number of data paths per chip based on it's lower power and die size requirements

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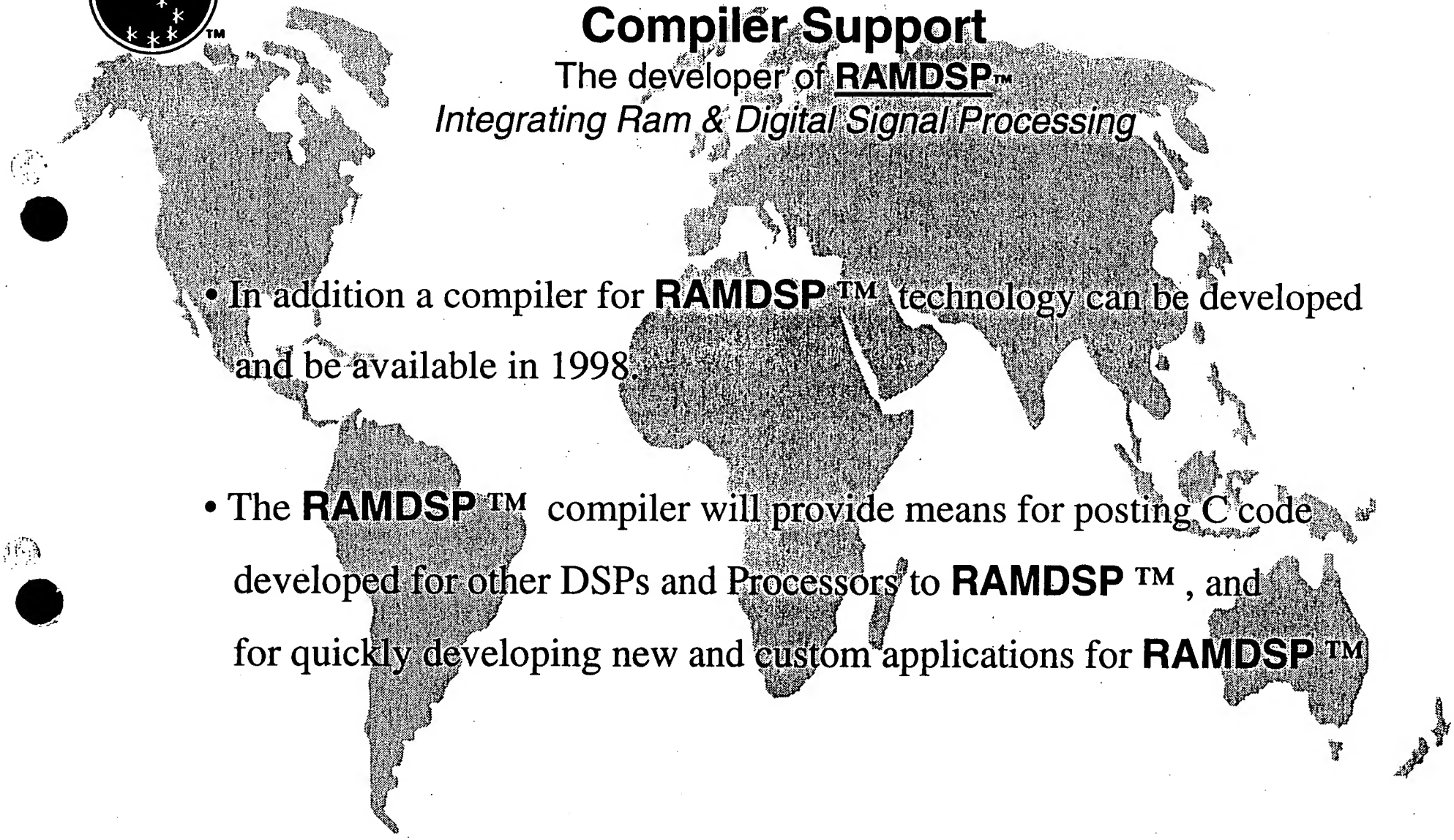
Stellar Architecture

Compiler Support

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- In addition a compiler for **RAMDSP ™** technology can be developed and be available in 1998.

- The **RAMDSP ™** compiler will provide means for posting C code developed for other DSPs and Processors to **RAMDSP ™** , and for quickly developing new and custom applications for **RAMDSP ™**

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Stellar Architecture

Additional Important Benefits

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Elimination of complex IOP (I/O Processor)
- Advanced techniques for reconfiguring and sharing DRAM and SRAM memory
- Memory management of DRAM and SRAM results in seamless execution of complex DSP applications
  - delays due to DMA or I/O are overlapped with computation
- Minimization of on-chip silicon for addressing and control of DRAM, while maintaining high-bandwidth communications to RAM

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Stellar Architecture

Additional Important Benefits

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

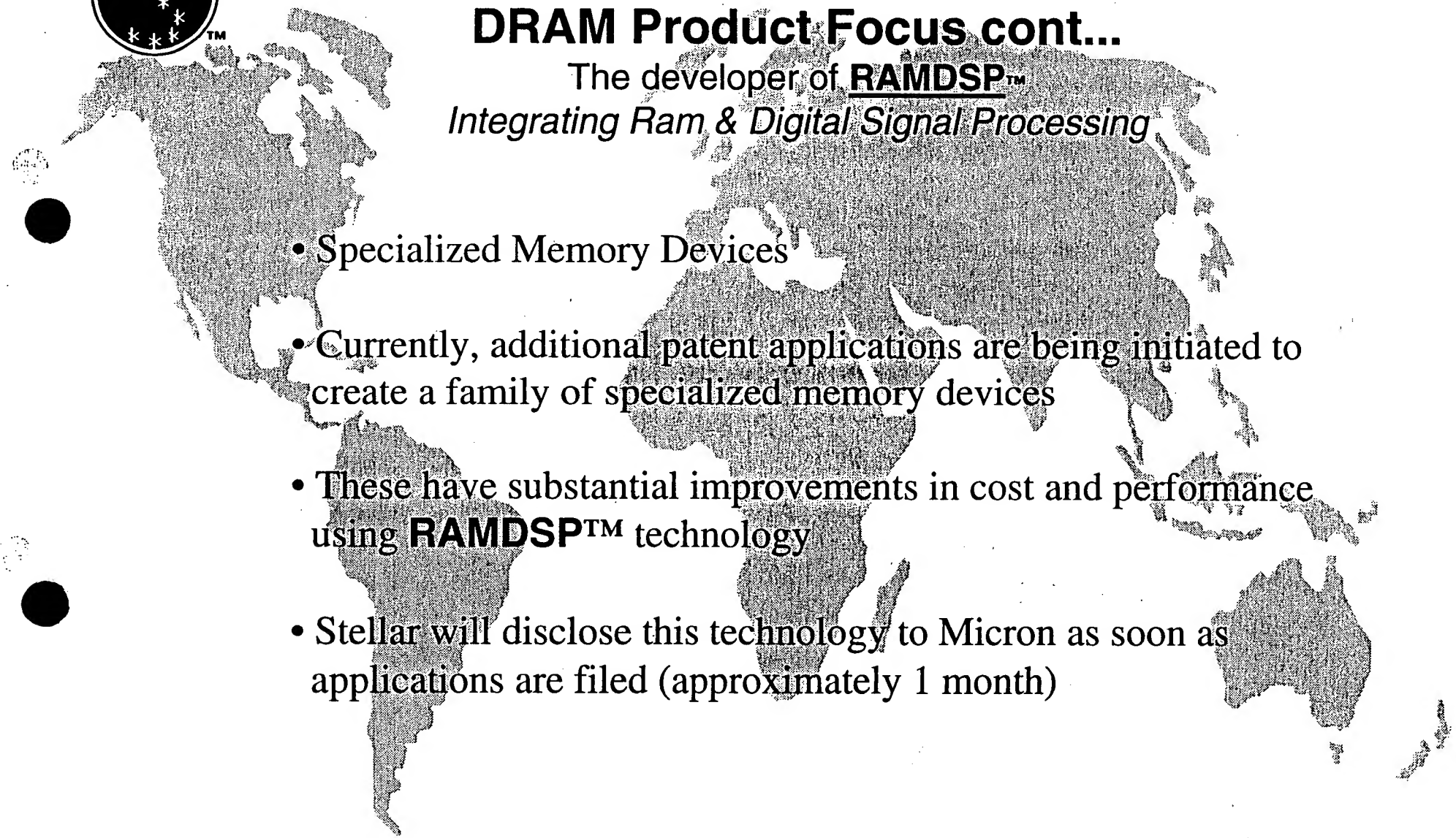
- Minimal size of memory structure (cell area), while supporting high-throughput execution
- Requirements for moving data between multiple engines and memory blocks substantially reduced
- Low power designs inherent in **RAMDSP™** architecture
- Reconfiguration capabilities for single and multiple engine applications

Stellar Products

DRAM Product Focus cont...

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



- Specialized Memory Devices
- Currently, additional patent applications are being initiated to create a family of specialized memory devices
- These have substantial improvements in cost and performance using **RAMDSP™** technology
- Stellar will disclose this technology to Micron as soon as applications are filed (approximately 1 month)

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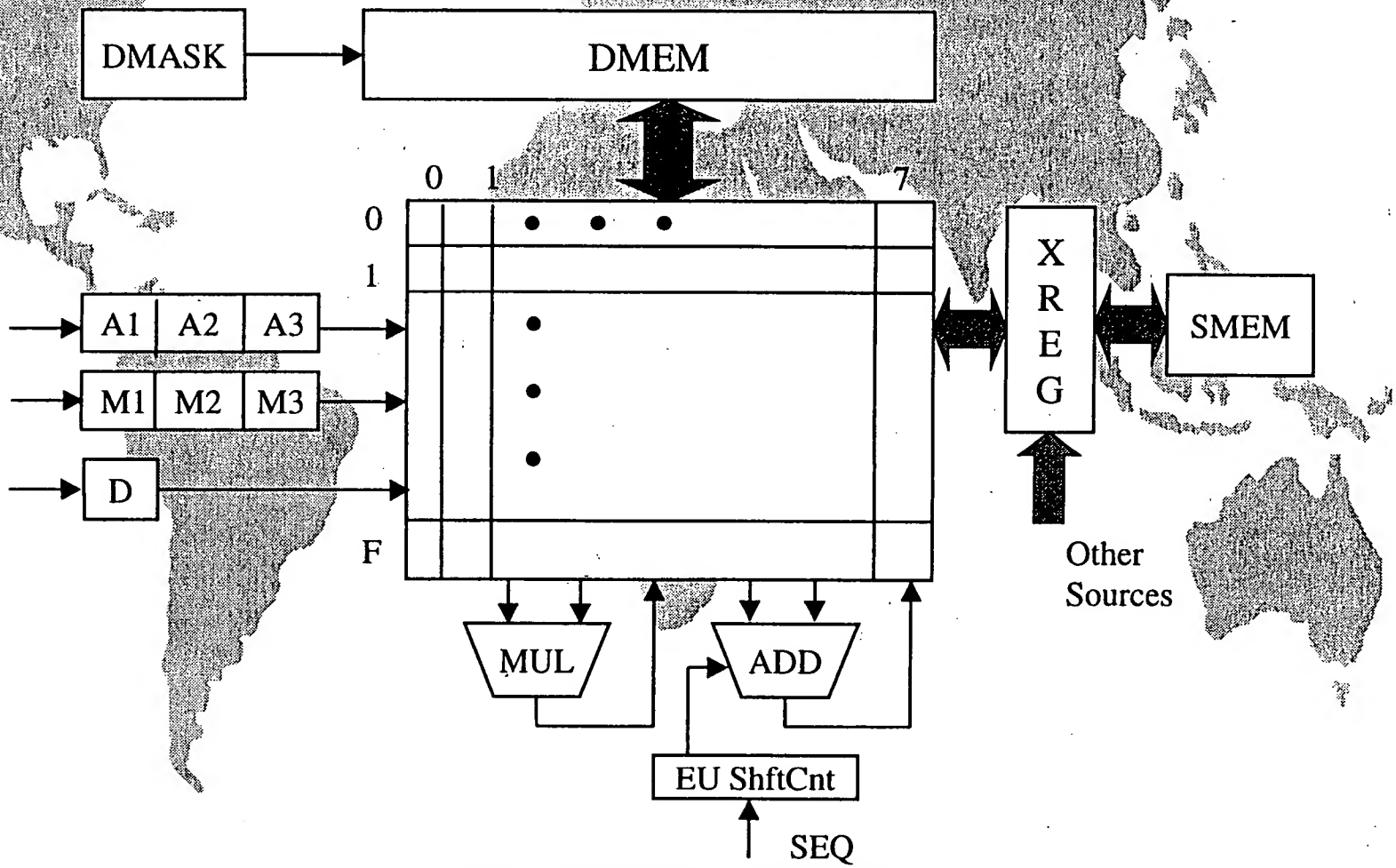
Stellar Architecture

Execution Unit Detail

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

RAMDSP applied to Video Applications

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Low power solution to upcoming generation of digital-video consumer products
  - Professional Broadcasting
  - PCs and Workstations
  - DVD-based Video Recorders and Camcorders
- Key enablers to new technologies
  - Design Flexibility
  - Programmability
  - Integrated Memory

Stellar Architecture

RAMDSP Design Flexibility Targets MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- EU design can be "bulked up" when applied to simple operations such as those used in motion estimation.
- Motion Estimation can require up to 8 Gops of performance or more.
- EU performance scales upward and is only limited by DRAM bandwidth.

Stellar Architecture

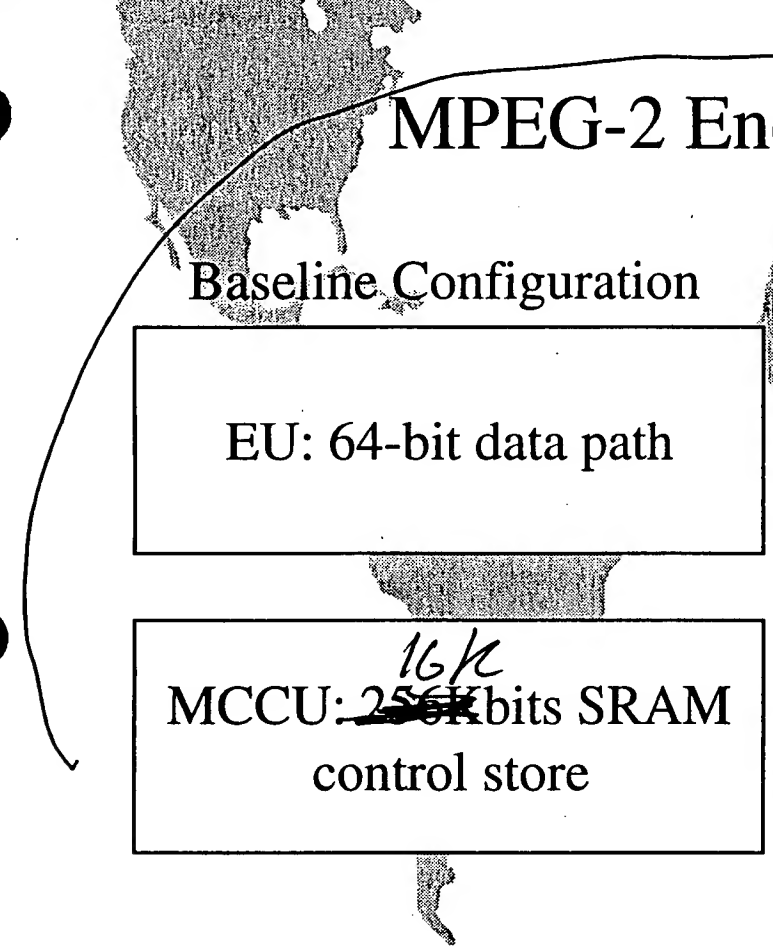
RAMDSP Design Flexibility Targets MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

MPEG-2 Encoder Motion Estimation

Baseline Configuration	ME Configuration
EU: 64-bit data path	EU: 128,256-bit data path
MCCU: ~~256K~~ 16K bits SRAM control store	MCCU: ~~128-64K~~ 16K bits ~~SRAM control store~~

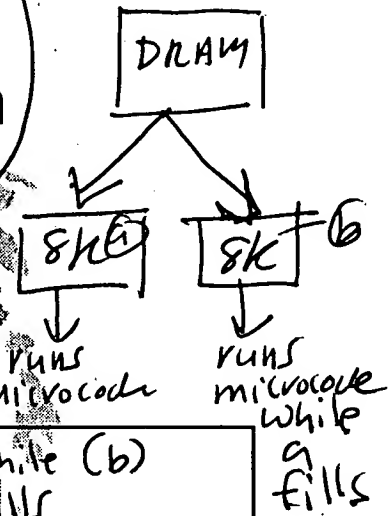


Stellar Architecture

RAMDSP MPEG-2 Encoder Solution

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Single Chip Solution

Codec Unit BIU: Bitstream Capable EU: 64-bit data path	Motion Estimation Unit EU: 128-bit data path
Motion Estimation Unit EU: 128-bit data path	Motion Estimation Unit EU: 128-bit data path

Stellar Architecture

RAMDSP Programmability Targets MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

MPEG-2 Motion Estimation Algorithms

EU: $\sum_{m=0}^{15}\sum_{n=0}^{15} | X_{m,n} - R_{m+i,n+j} |$

$\sum_{m=0}^{7}\sum_{n=0}^{15} | X_{m,n} - R_{m+i,n+j} |$

$\sum_{m=0}^{15}\sum_{n=0}^{15} | X_{m,n} - \frac{(R_{m+i,n+j} + R_{m+i,n+j+1})}{2} |$

$\sum_{m=0}^{15}\sum_{n=0}^{15} (X_{m,n} - R_{m+i,n+j})^2$

...

MCCU: Three-step search
Hierarchical search
Full search

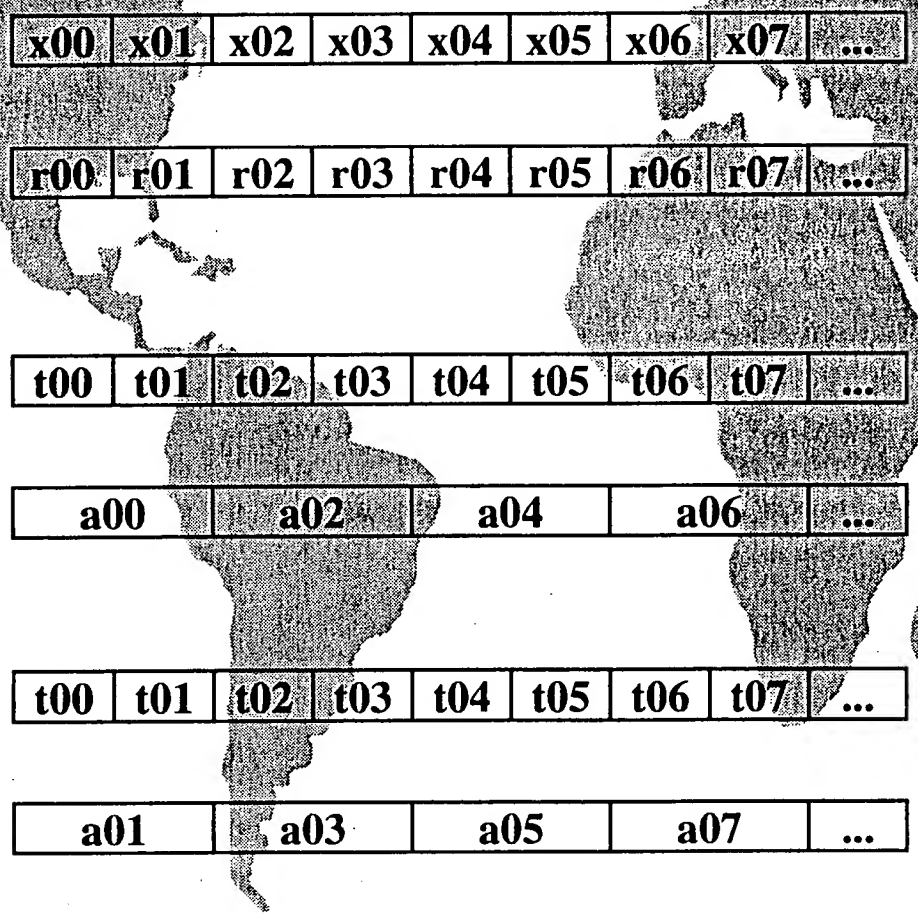
...

Stellar Architecture

RAMDSP Programmability Targets MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



$$t_{ij} = abs\,(x_{ij} - r_{ij})$$

(8) 8-bit ops

$$a_{ij} = a_{ij} + t_{ij}$$

(4) 16-bit ops

$$a_{ij} = a_{ij} + t_{ij}$$

(4) 16-bit ops

Stellar Architecture

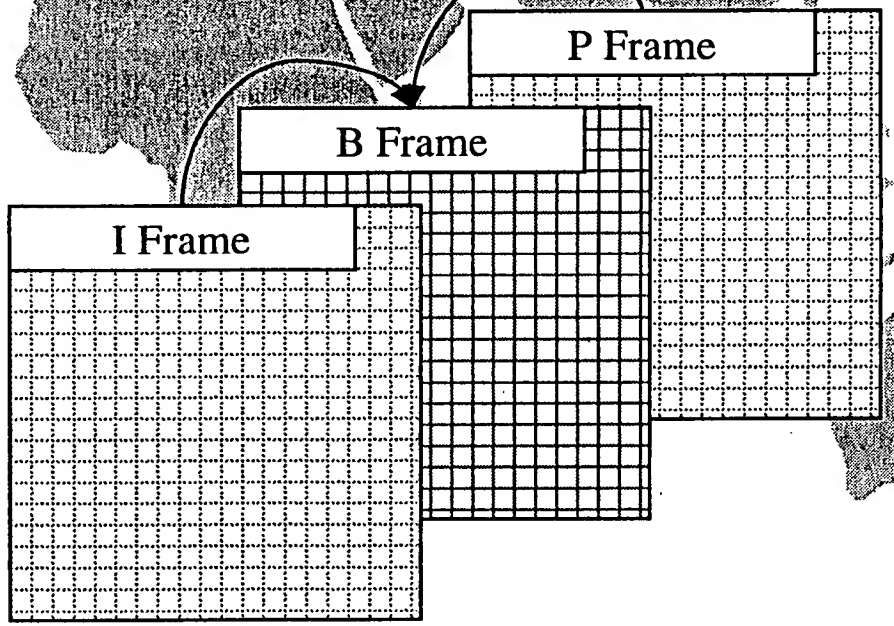
RAMDSP Integrated Memory Targets MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Motion Estimation Buffer Requirements

RAMDSP ™ features multiple Mbytes of memory resident near the execution unit, which allows quick access to predictor frames.



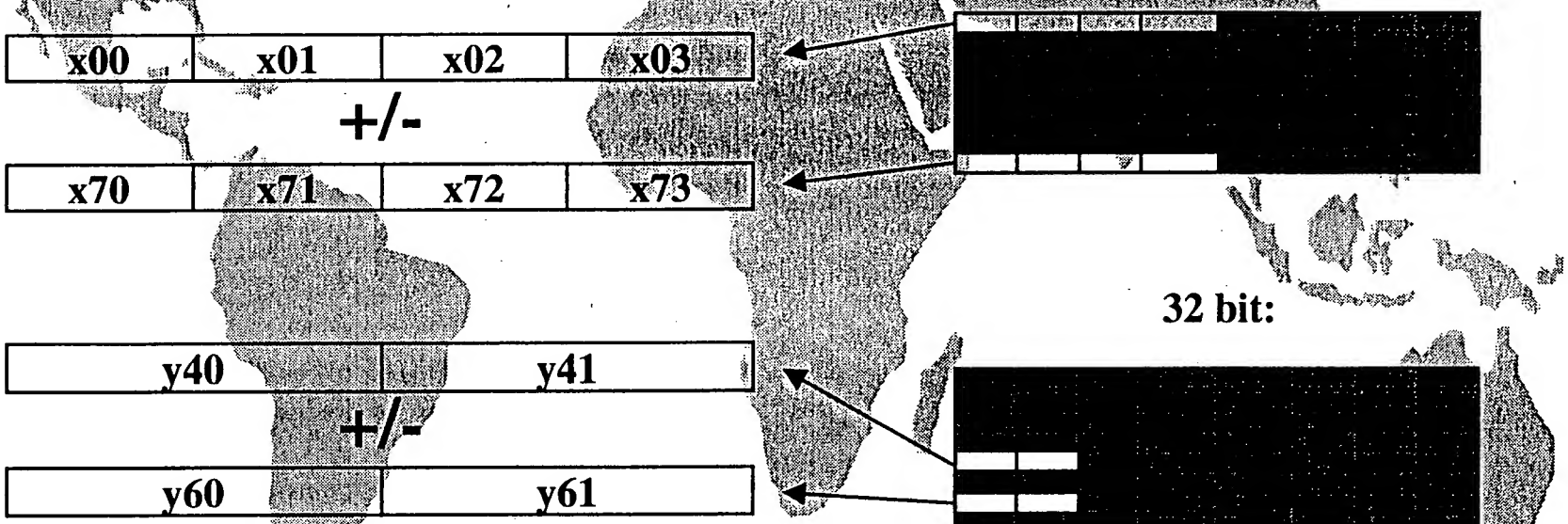
Stellar Architecture

RAMDSP Performance on 8x8 DCT

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Depending on the data type, EU can operate on 4 or 2 columns at a time, per 64-bit data path



Stellar Architecture

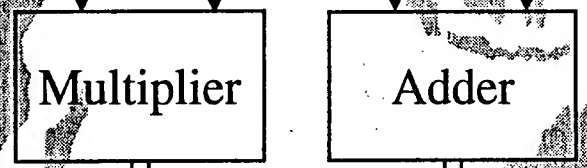
RAMDSP Performance on 8x8 DCT

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Fast transpose operation keeps SIMD style column operations running at near-peak performance

x00	x01	x02	x03
x10	x11	x12	x13
x20	x21	x22	x23
x30	x31	x32	x33



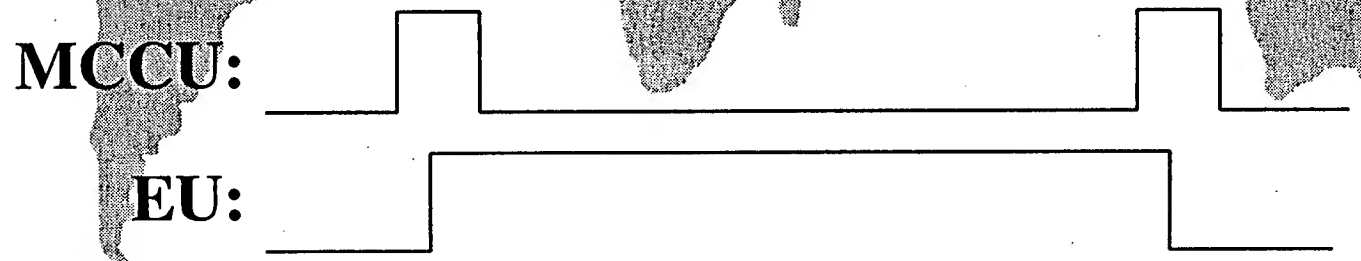
x00	x10	x20	x30
x01	x11	x21	x31
x02	x12	x22	x32
x03	x13	x23	x33

Stellar Architecture

RAMDSP Performance on 8x8 DCT

The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing

- A single 8x8 DCT operation takes approximately 200 clock cycles on a 64-bit EU datapath.
- Assuming an 8:1 ratio between EU cycle times and DRAM cycle times, and a 512-bit wide data bus:
  - DRAM cycles to load data from memory: 2
  - DRAM cycles to compute the 8x8 DCT: 25
  - DRAM cycles to store data to memory: 2



Stellar Architecture

RAMDSP Bus Interface Unit for MPEG-2

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

- Bus Interface Unit from baseline configuration is enhanced to facilitate bitstream coding and decoding.
  - Fast SRAM added for quick coefficient lookup, and access to quantizer matrices.
  - Additional shift operations, leading one operations.
  - Caching of data to aid in zigzag ordering before storing to DRAM, or writing to bus.

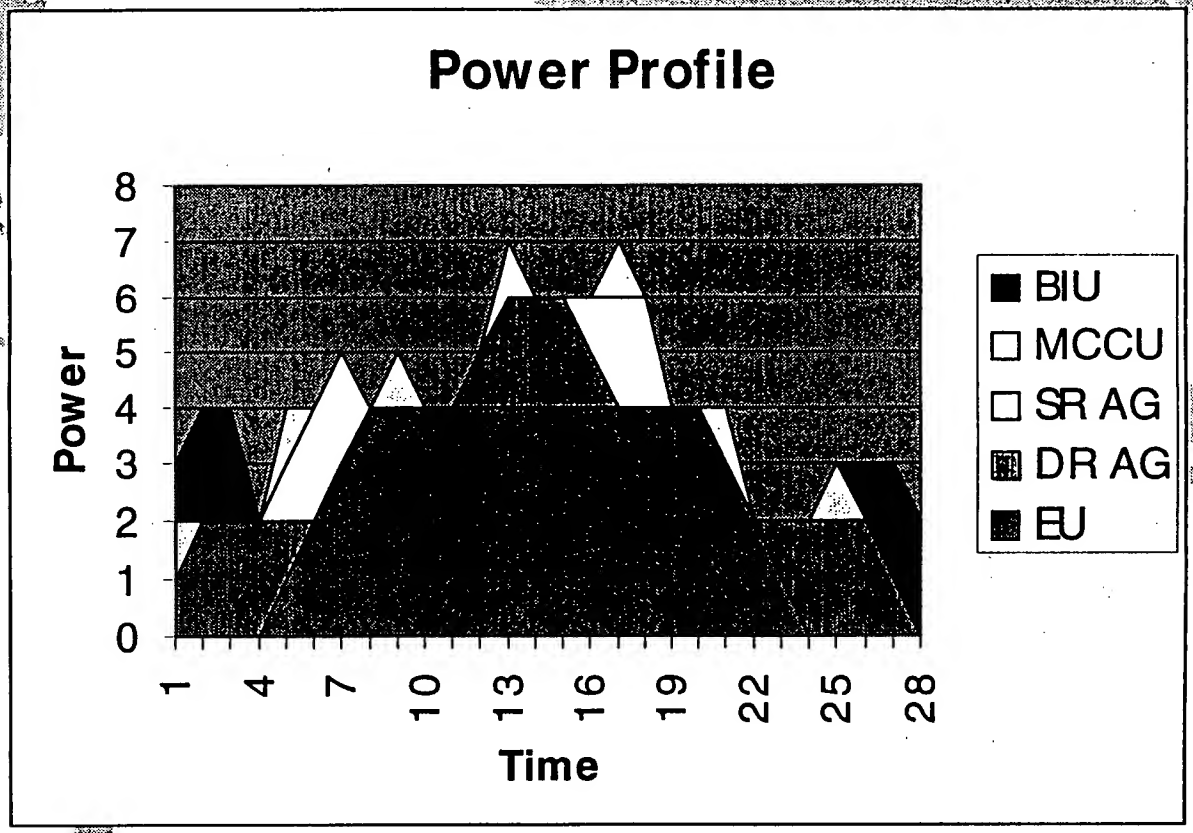
09

Stellar Architecture

Power Profile

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing



Stellar Architecture

RAMDSP vs. Other MPEG-2 Encoder Solutions

The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing

	CHROMATIC MPACT 2	C-CUBE DVX	TRIMEDIA TM-1000	RAMDSP 3+1
Architecture	**VLIW ME CoProc**	**DSPCore RISC Core ME CoProc**	**VLIW Decode Core**	**SIMD - Vector**
Transistors	**3.0 M**	**5.5 M**	**5.5 M**	**2.0 M**
Peak Performance	**6 Bops**	**1 Bop + ME**	**3.8 Bops**	**11 Bops**
Memory Configuration	**4 – 8 MB RAMBUS**	**8 MB SDRAM**	**SDRAM**	**8 MB emedded**
Notes	**Toshiba may embed 4MB DRAM**		**MPEG-2 decode only**	

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Stellar Architecture

RAMDSP Device Count Estimation for MPEG Application

The developer of **RAMDSP™**

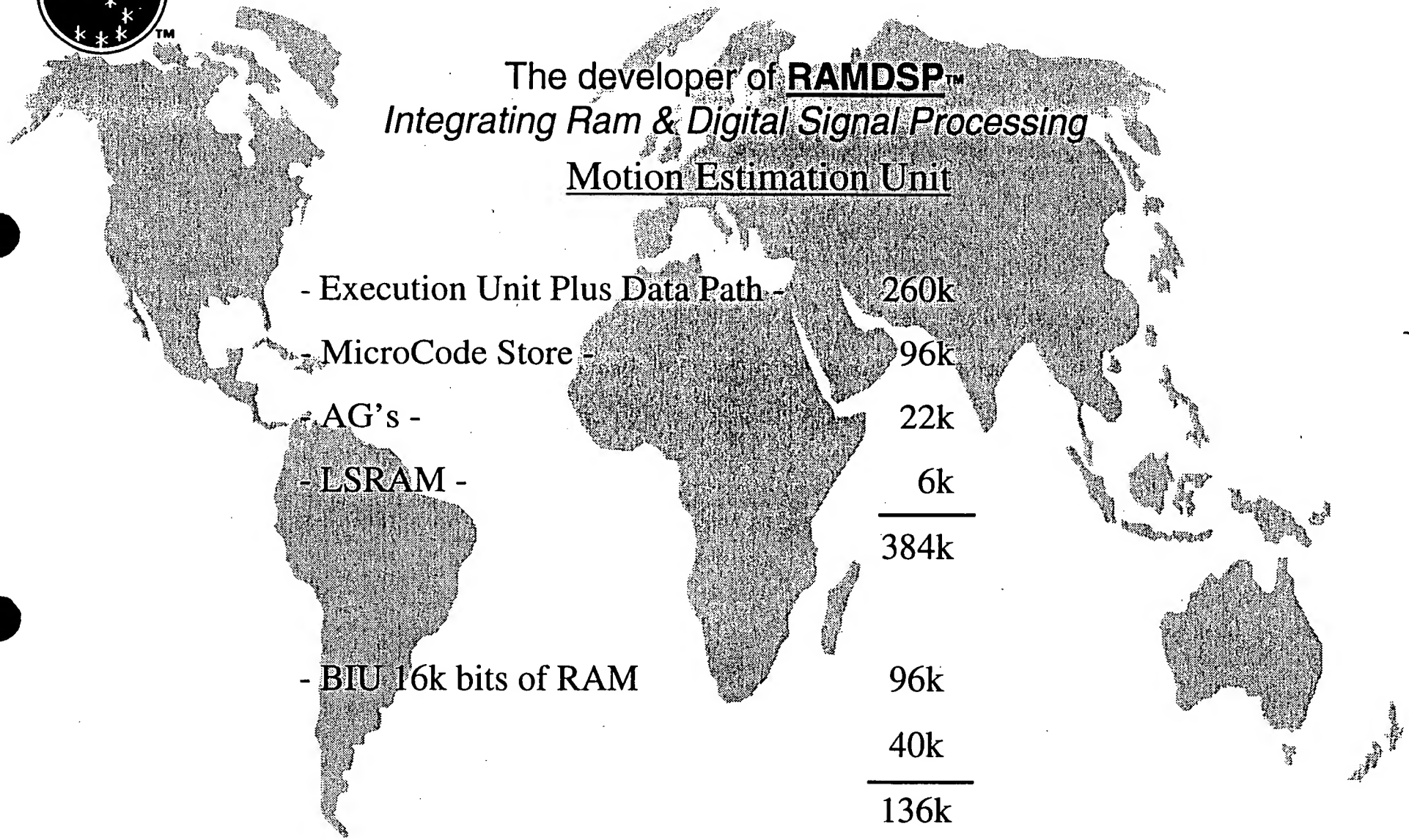
Integrating Ram & Digital Signal Processing

Execution Unit plus Data Path	
Register File	160k
Data Path	~ 50k
MicroCode Store	
16k SRAM -	96k Transistors
Address Generators and Controllers	
SE AG	~ 5k
DMA AG	~ 6.5k
DMEM AG	~ 6.5k
LMEM AG	~ 4.0k

NOTE: THAT A THREE LEVEL PIPE LINE IN THE EXECUTION DATA PATH WOULD IMPROVE PERFORMANCE SO THAT ONE ME ENGINE could be Eliminated thus a reduction of 500,000 TRANSISTORS up.

03

Stellar Architecture



The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Motion Estimation Unit

- Execution Unit Plus Data Path -	260k
- MicroCode Store -	96k
- AG's -	22k
- LSRAM -	6k
	384k
- BIU 16k bits of RAM	96k
	40k
	136k

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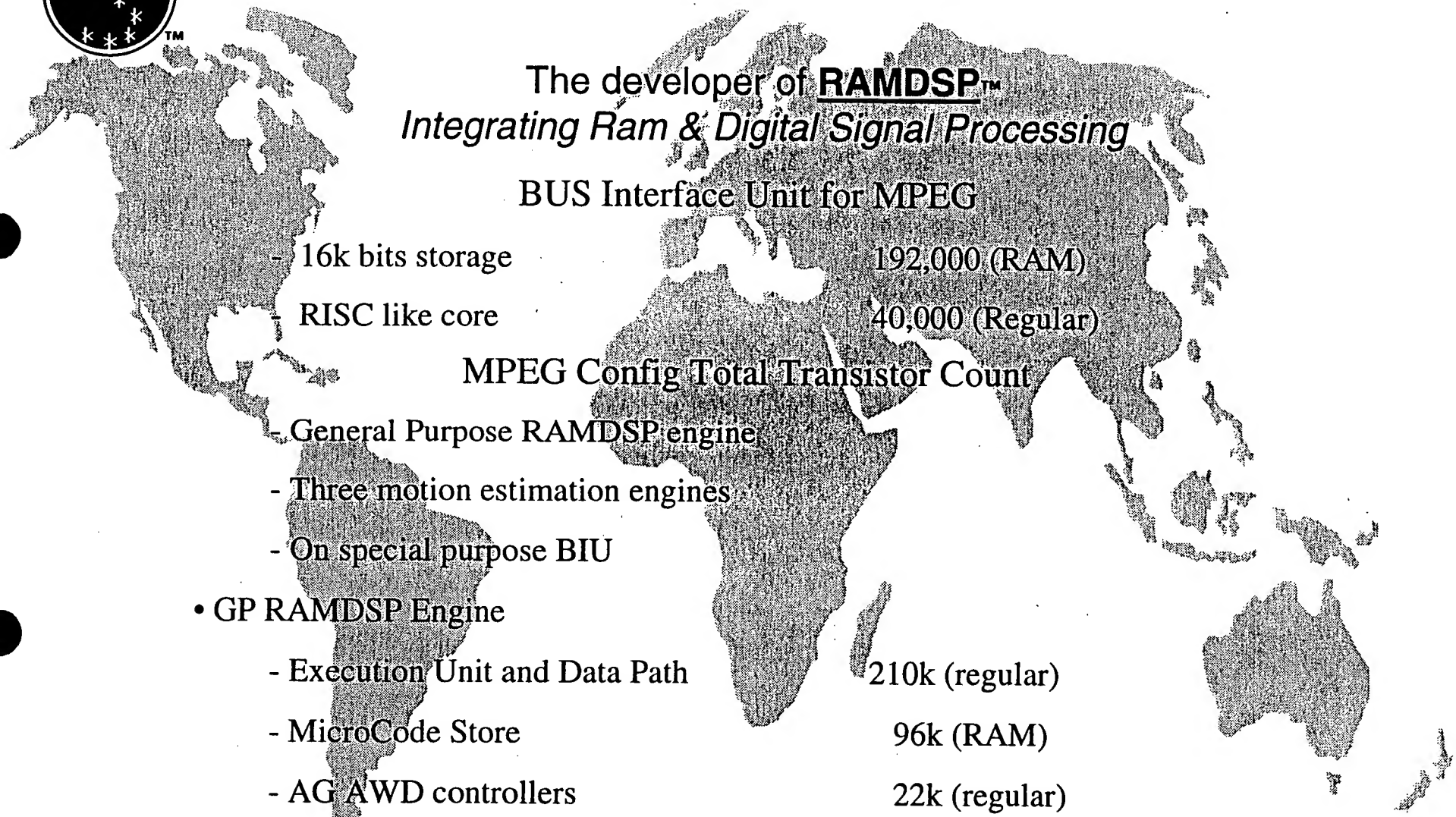
Stellar Architecture



The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

BUS Interface Unit for MPEG

- 16k bits storage — 192,000 (RAM)
- RISC like core — 40,000 (Regular)

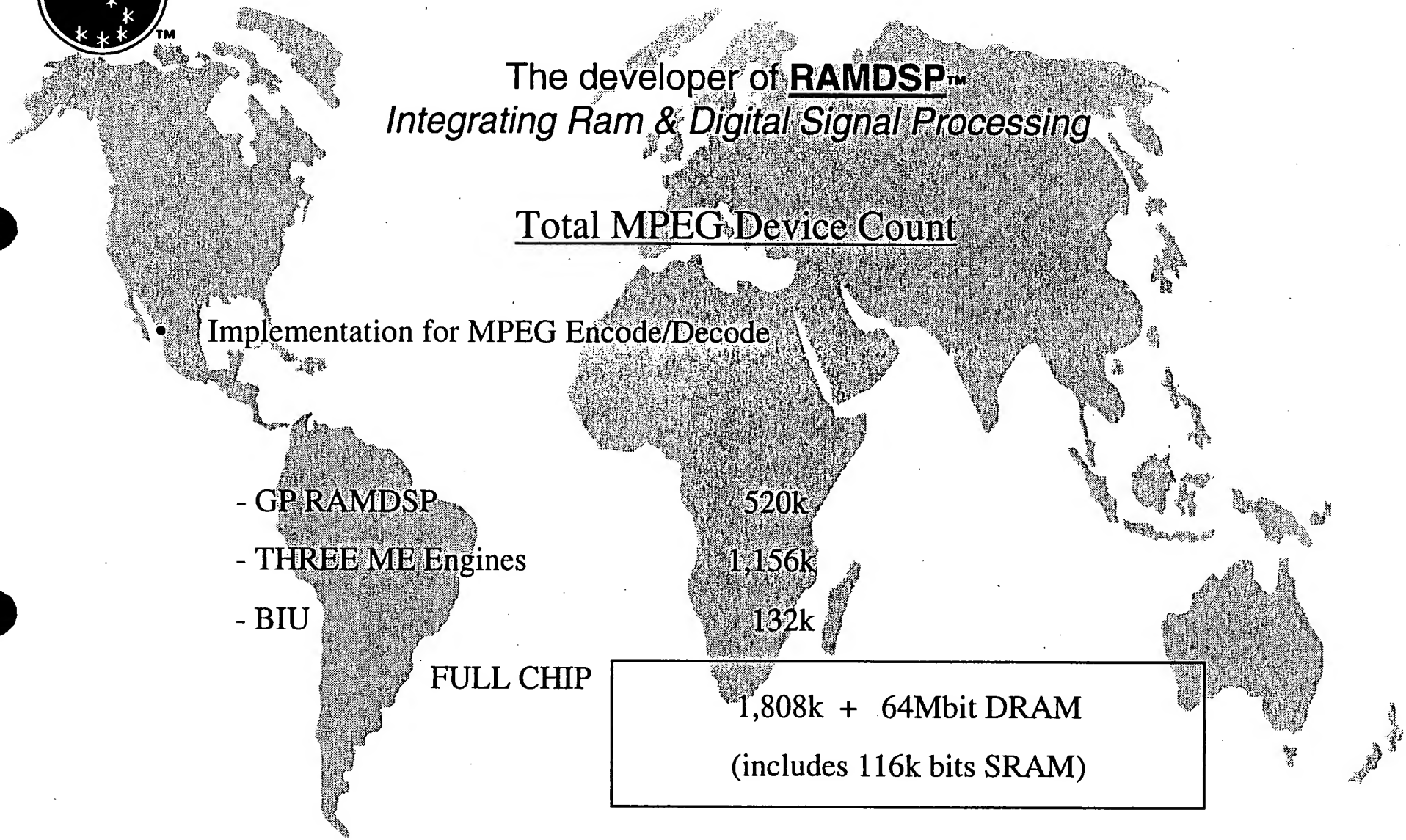
MPEG Config Total Transistor Count

- General Purpose RAMDSP engine
- Three motion estimation engines
- On special purpose BIU

• GP RAMDSP Engine

- Execution Unit and Data Path	210k (regular)
- MicroCode Store	96k (RAM)
- AG AWD controllers	22k (regular)
- LSRAM - (32k bits)	192k (RAM)
	520 k

Stellar Architecture



The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

Total MPEG Device Count

- Implementation for MPEG Encode/Decode

- GP RAMDSP	520k
- THREE ME Engines	1,156k
- BIU	132k
FULL CHIP	1,808k + 64Mbit DRAM (includes 116k bits SRAM)

SEQ and AG instructions

UNIT				op code	operand 1	operand 2
	nop			00000000		
SEQ	halt			00000001		
SEQ	return			00000010		
SEQ	jmp	s		00010000	4 bits	
SEQ	call	s		00010001	4 bits	
	putx	s		00010010	4 bits	
	getx	d		00010011	4 bits	
	putxhi	s		00010100	4 bits	
	getxhi	d		00010101	4 bits	
SEQ	getstat	d		00010110	4 bits	
SEQ	setshft	s		00010111	4 bits	
SEQ	setcfg	s		00011000	4 bits	
SEQ	setloop	s		00011001	4 bits	
SEQ	setcond	s		00011010	4 bits	
	inc	d		0010000x	4 bits	
	dec	d		0010001x	4 bits	
	add	s	d	0011000x	4 bits	4 bits
	sub	s	d	0011001x	4 bits	4 bits
	neg	s	d	0011010x	4 bits	4 bits
	mov	s	d	0011011x	4 bits	4 bits
	and	s	d	0011100x	4 bits	4 bits
	or	s	d	0011101x	4 bits	4 bits
	xor	s	d	0011110x	4 bits	4 bits
	not	s	d	0011111x	4 bits	4 bits
	shft	cnt	d	010000	6 bits	4 bits
SEQ	brcond	offset		0110	12 bits	
SEQ	loop	offset		0111	12 bits	
AG	setavec	val		0110	12 bits	
AG	setmvec	val		0111	12 bits	
	ldi	val	d	10	10 bits	4 bits
	ldiu	val	d	11	10 bits	4 bits

Note: If x = 1, then set the DRAM address register with the ALU output.

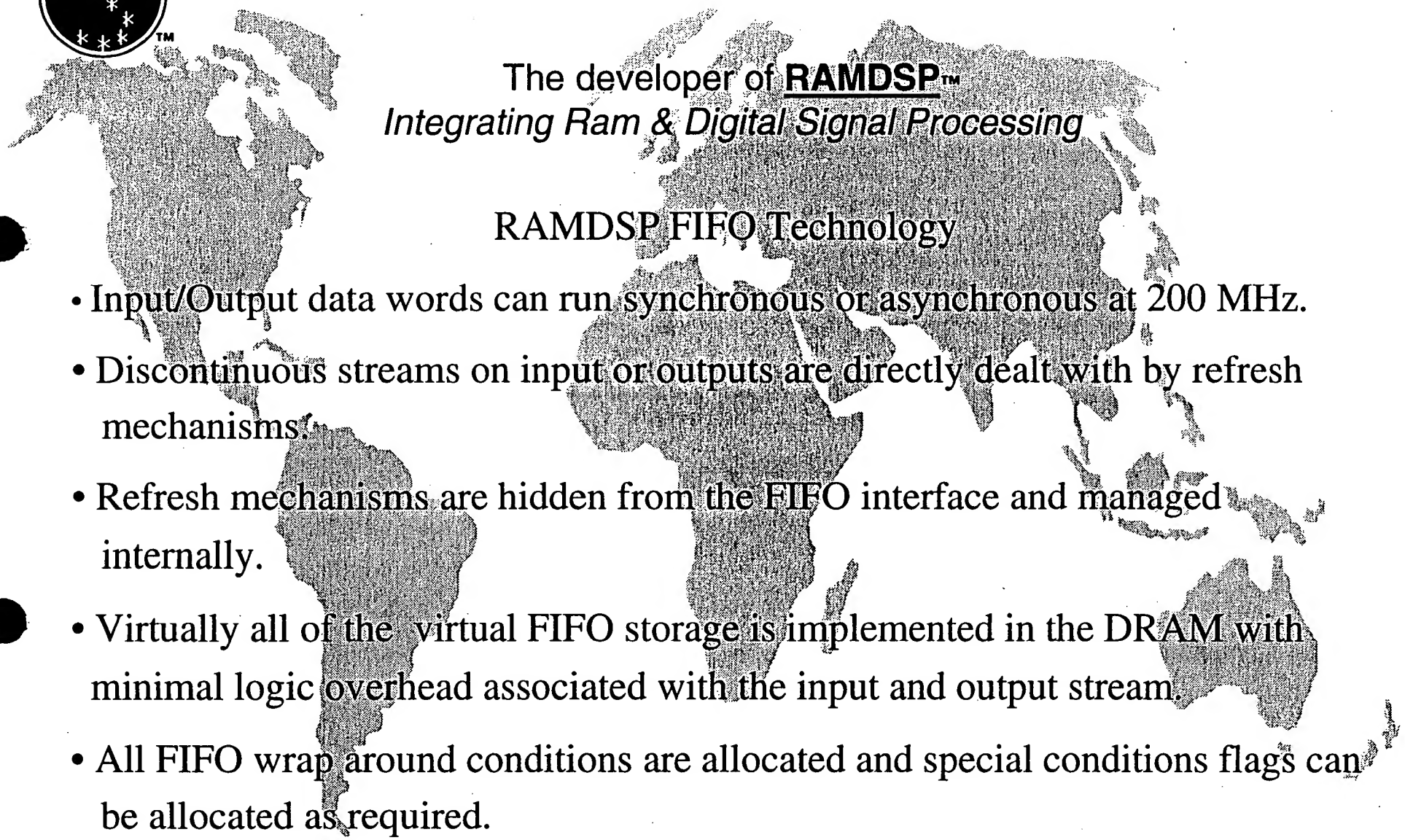
EU Adder instructions

anop							0000000			
pacc	u/s	h/l	8/16		s	d	0001111	uhz	3 bits	3 bits
padd	u/s	sat/non	8/16/32	s1	s2	d	001uszz	3 bits	3 bits	3 bits
psub	u/s	sat/non	8/16/32	s1	s2	d	010uszz	3 bits	3 bits	3 bits
pabdif	u/s	sat/non	8/16/32	s1	s2	d	011uszz	3 bits	3 bits	3 bits
pars	u/s	sat/non	8/16/32	s1	s2	d	100uszz	3 bits	3 bits	3 bits
pcomp	u/s	sat/non	8/16/32	s1	s2	d	101uszz	3 bits	3 bits	3 bits
pshft	u/s	sat/non	8/16/32/64	s1	s2	d	110uszz	3 bits	3 bits	3 bits
pldzero			8/16/32/64		s	d	11100zz		3 bits	3 bits
pldone			8/16/32/64		s	d	11101zz		3 bits	3 bits
cshft				s1	s2	d	1111000	3 bits	3 bits	3 bits
dshft				s1	s2	d	1111001	3 bits	3 bits	3 bits
and				s1	s2	d	1111010	3 bits	3 bits	3 bits
or				s1	s2	d	1111011	3 bits	3 bits	3 bits
xor				s1	s2	d	1111100	3 bits	3 bits	3 bits
not					s	d	1111101		3 bits	3 bits

EU Multiplier instructions

mnop							0000000			
ppack	u/s	h/l	16/32,sat		s	d	000100s	uhz	3 bits	3 bits
punpk	u/s	h/l	8/16		s	d	0001010	uhz	3 bits	3 bits
pacc2	u/s	h/l	8/16		s	d	0001111	uhz	3 bits	3 bits
padd2	u/s	sat/non	8/16/32	s1	s2	d	001uszz	3 bits	3 bits	3 bits
psub2	u/s	sat/non	8/16/32	s1	s2	d	010uszz	3 bits	3 bits	3 bits
pabdif2	u/s	sat/non	8/16/32	s1	s2	d	011uszz	3 bits	3 bits	3 bits
pars2	u/s	sat/non	8/16/32	s1	s2	d	100uszz	3 bits	3 bits	3 bits
pmul	u/s	hh/ll/hl/lh	8/16	s1	s2	d	101uhhz	3 bits	3 bits	3 bits
pmin	u/s		8/16/32/64	s1	s2	d	1100uzz	3 bits	3 bits	3 bits
pmax	u/s		8/16/32/64	s1	s2	d	1101uzz	3 bits	3 bits	3 bits
cndmrg			8/16/32	s1	s2	d	11100zz	3 bits	3 bits	3 bits
cndmov			8/16/32		s	d	11101zz		3 bits	3 bits

Stellar Architecture

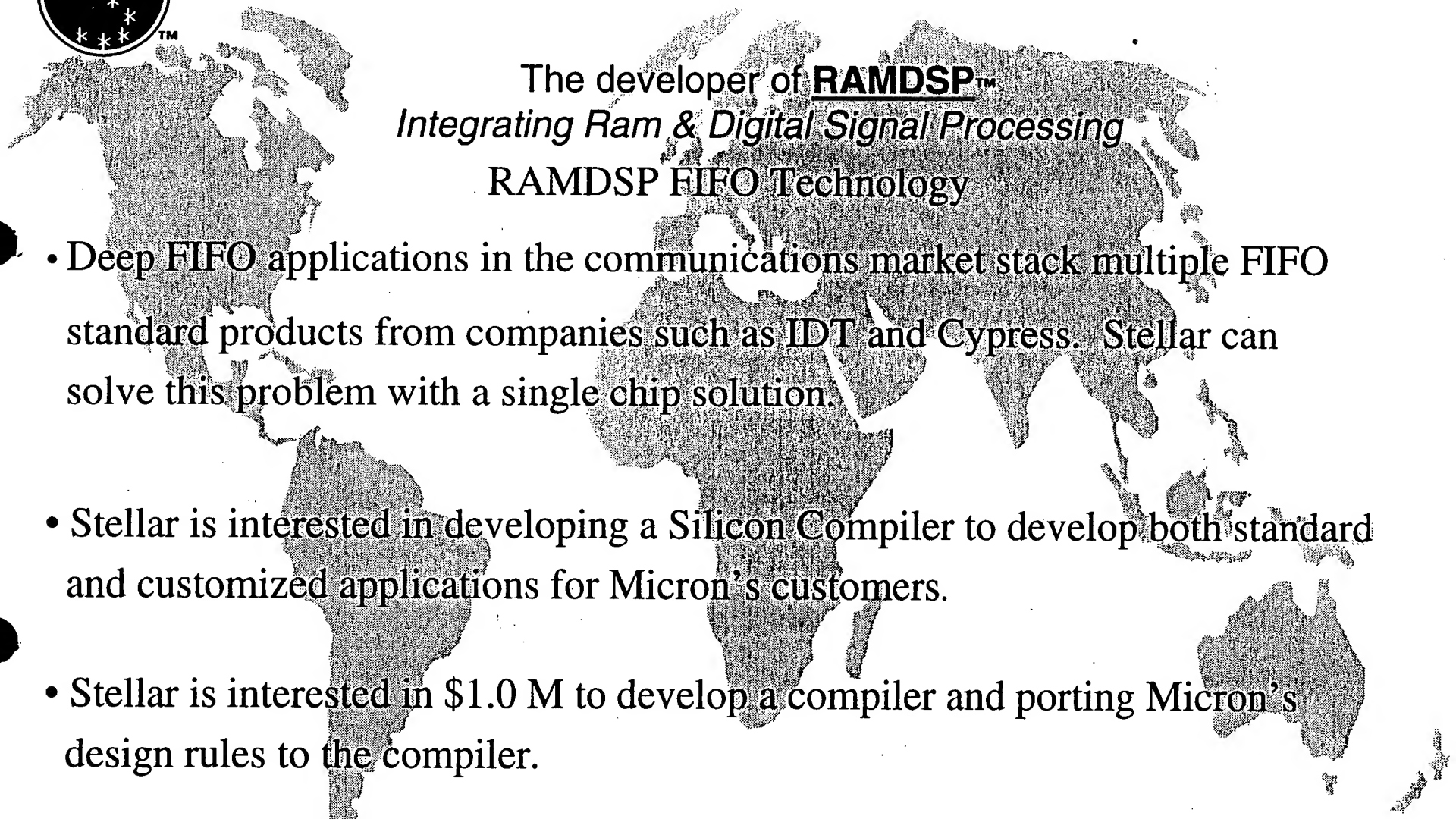


The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing

RAMDSP FIFO Technology

- Input/Output data words can run synchronous or asynchronous at 200 MHz.
- Discontinuous streams on input or outputs are directly dealt with by refresh mechanisms.
- Refresh mechanisms are hidden from the FIFO interface and managed internally.
- Virtually all of the virtual FIFO storage is implemented in the DRAM with minimal logic overhead associated with the input and output stream.
- All FIFO wrap around conditions are allocated and special conditions flags can be allocated as required.

Stellar Architecture



The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing
RAMDSP FIFO Technology

- Deep FIFO applications in the communications market stack multiple FIFO standard products from companies such as IDT and Cypress. Stellar can solve this problem with a single chip solution.

- Stellar is interested in developing a Silicon Compiler to develop both standard and customized applications for Micron's customers.

- Stellar is interested in $1.0 M to develop a compiler and porting Micron's design rules to the compiler.

- Payment is based upon pre-paid one time license fee and pre-paid royalties.

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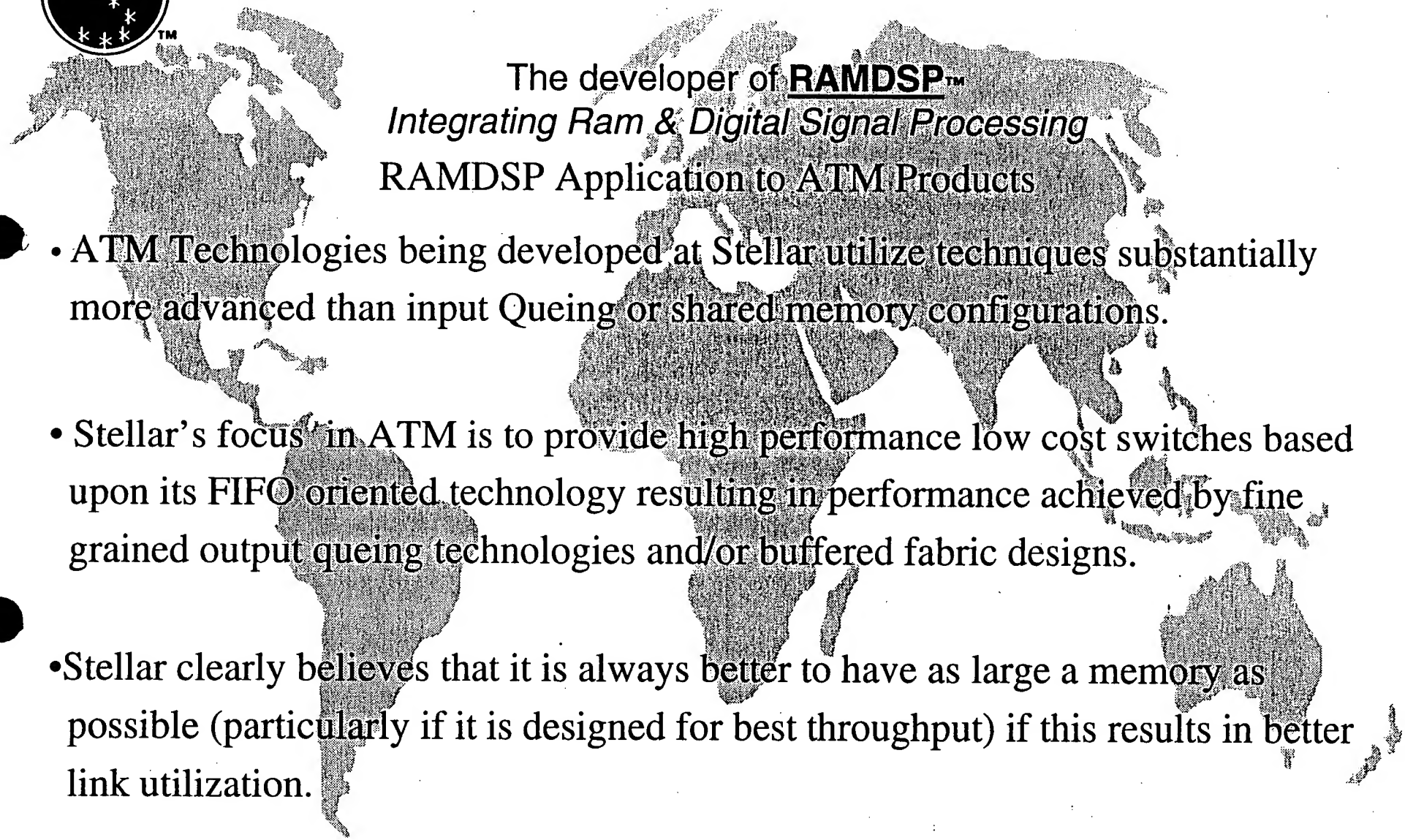
Stellar Architecture



The developer of **RAMDSP™**
Integrating Ram & Digital Signal Processing

RAMDSP Application to ATM Products

- ATM Technologies being developed at Stellar utilize techniques substantially more advanced than input Queing or shared memory configurations.

- Stellar's focus in ATM is to provide high performance low cost switches based upon its FIFO oriented technology resulting in performance achieved by fine grained output queing technologies and/or buffered fabric designs.

- Stellar clearly believes that it is always better to have as large a memory as possible (particularly if it is designed for best throughput) if this results in better link utilization.

Stellar Architecture

The developer of **RAMDSP™**

Integrating Ram & Digital Signal Processing

RAMDSP Application to ATM Products

- Stellar switching technology will also address multicasting requirements for Internet and ATM network.

- In addition tight coupling between Stellar's switch technology and RAMSDP technology will support the emergence of non-blocking switching backbone coupled with tight coupling to the signal process environment, e.g. -- coupling to Stellar MPEG technologies, and other RAMDSP Signal Processing.